Fault generated noise protection for complex EHV systems

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FAULT GENERATED NOISE PROTECTION FOR COMPLEX EHV SYSTEMS

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SUMMARY

More complicated network configurations are starting to be encountered on Extra High Voltage (EHV) transmission systems. However, they may require complicated and expensive protection schemes to adequately protect them. This thesis presents a new technique for accurately detecting faults on EHV teed and composite circuits. Fault generated high frequency (HF) voltage signals are extracted from the coupling capacitor of a standard capacitor voltage transformer with a specially designed circuit. A very high sampling rate is used to capture these signals which are then manipulated using digital signal processing techniques.

Power line carrier line traps are used to confine the HF signals to the protected zone and their bandstop characteristics are used as a basis for discriminating between internal and external faults. It is essentially a non-unit technique as it only uses locally derived information but it has the discriminative properties normally associated with unit protection schemes. Therefore, it does not need any expensive communication channels which can compromise the security of some unit protection schemes if they fail.

Simulated results are presented for a variety of internal and external faults on several different complex networks. These show that the technique is capable of discriminating between internal and external faults in less than approximately five milliseconds. It is not adversely affected by factors such as fault type, position or inception angle. Any influence of the capacities of the connected sources is minimised by the strong barrier formed by the line trap and busbar stray capacitance at high frequencies.

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LIST OF SYMBOLS AND ABBREVIATIONS

ACSR	Aluminium Conductor Steel Reinforced
A/D	Analogue to Digital
a_n, b_n	Digital filter coefficients
C	Shunt capacitance per unit length
C_1, C_2, L_1, L_2, R_1	Line trap parameters
C_c	Coupling capacitor
C_p, L_p, R_p	Stack tuner parameters
C_s	Busbar stray capacitance
CAD	Computer Aided Design
CASE	Co-operative Award in Science and Engineering
CT	Current Transformer
CVT	Capacitor Voltage Transformer
D_r	Discrimination ratio
dc	Direct current
EHV	Extra High Voltage
EMTP	ElectroMagnetic Transients Program
EPSRC	Engineering and Physical Sciences Research Council
$f_1(t-\alpha x)$	Forward travelling wave function
$f_2(t+\alpha x)$	Backward travelling wave function
g	Time varying arc conductance

G	Stationary arc conductance
G_o	Digital filter gain
$H(z)$	Digital filter transfer function
HF	High Frequency
I	Phase current vector
I^c	Modal current vector
I_M	Arc current magnitude
IIR	Infinite Impulse Response
k	Summation variable
ℓ	Time dependent arc length
L	Series inductance per unit length
L_{av}	Moving average filter length
L_s	CVT inductance
n	Time step number
NGC	National Grid Company
P	Matrix whose Eigenvectors are the Modal propagation constants
P, Q, R	Line ends
P_m	Mean power
PLC	Power Line Carrier
Q	Modal current matrix
R	Resistive component per unit arc length
R_s	Source resistance
s	Laplace domain operator

S	Modal voltage matrix
SVA	Source short circuit level
t	Time
Δt	Sampling interval
t_f	Fault inception time
T	Time limit
$T(s)$	Analogue filter transfer function
TACS	Transient Analysis of Control Systems
V	Phase voltage vector
V_a, V_b, V_c	Phase voltages
V^c	Modal voltage vector
V_{fx}	Bandpass filter output
V_L	Line voltage
V_o	Constant voltage parameter per unit arc length
V_x, V_y	Modal voltages
VT	Voltage Transformer
x	Distance
$x(t)$	Time domain signal
X : R	Source impedance ratio
X_s	Source reactance
Y	Admittance matrix
$Y(n\Delta t)$	Enhanced filter output
z	Z domain operator
Z	Impedance matrix

Z_L	Distance relay impedance setting
Z_o	Line characteristic impedance
Z_s	Source impedance
Z_{s0}:Z_{s1}	Source zero phase sequence to positive phase sequence impedance
$1/\alpha$	Surge velocity
θ	Line impedance angle
τ	Arc time constant

CHAPTER 1

INTRODUCTION

1.1 Electricity Generation and Transmission

Electricity has become an essential item in the modern way of life and large industrial countries consume vast amounts of electrical power. It is not economical for each consumer to produce their own electricity and so it is generated in large power stations which can typically produce over 500 MW of electrical power. Large amounts of power, therefore, need to be transmitted from the power stations to the individual consumers.

The losses encountered when transmitting electricity are associated with the ohmic heating of the conductors and so they can be minimised by keeping the current flow as low as possible. To maintain the ability to transmit the necessary power, the voltage must be raised. However, it is not practical to supply consumers with very high voltages and so a number of different voltage levels are required. In the United Kingdom, the generating stations supply a transmission network which operates at 275 kV and 400 kV. This network carries electricity to the regional distribution networks which supply electricity to the consumers after transforming the voltage

down a number of times. The transmission network therefore has a central role in supplying electricity.

A typical 400 kV transmission line can carry 1800 MVA which is enough electricity to supply a small town. Consequently, it is very important that the transmission system is not disrupted. The large amounts of energy involved in electricity transmission mean that faults have to be removed as quickly as possible for two main reasons; to minimise damage to power system equipment and to maintain electricity supplies.

1.2 Power System Faults

Power systems faults can be caused by a wide variety of reasons. Lightning strikes are the most common cause of faults and can affect transmission lines in different ways. The earth wire is designed to shield the phase conductors from lightning strikes, but if a conductor is struck, the induced overvoltage can cause a flashover across an insulator string. A strike on the earth wire does not always prevent a fault from occurring. A low magnitude surge may be induced which does not cause any problems, or the lightning strike may cause the potential of the nearest tower to rise sufficiently to cause a back flashover from the tower to a phase conductor initiating a fault. Once an ionised path has been formed, the phase voltage may maintain the fault as the tower potential decays to zero.

Faults can also be caused by equipment failure and objects getting too close to the power conductors. This includes branches of trees as well as man made items such as cranes. Fires underneath transmission lines can also cause a fault path to be formed. The hot air above the flames can become ionised and so form a conducting path. Many of these types of faults form a high impedance fault path and so only a relatively low fault current flows. These can be very difficult to detect using conventional methods and so may not be removed from the power system very rapidly.

Faults can involve any combination of conductors and can be clear of earth as well as being short circuited to earth. By far the majority of faults encountered in practice on transmission networks are single phase to earth faults. Three phase to earth and three phase clear of earth faults are the most severe, these can be caused by grounding wires being left on inadvertently after work has been carried out on the lines.

The objectives of power system protection are to detect the presence of these faults and to initiate the isolation of the affected equipment in the shortest possible time. However, it is vital that only the faulted item is isolated so that disruption to consumers is minimised.

This thesis presents a new technique for protecting extra high voltage (EHV) teed and composite transmission circuits by using fault generated high frequency voltage signals.

1.3 Thesis Structure

Chapter 2 gives some background information on power system protection. It describes conventional transmission circuit protection techniques, such as unit and non-unit schemes, as well as some of the more recent techniques. A description of the complex circuits dealt with in this thesis and their potential protection problems are presented.

Chapter 3 describes how the high frequency voltage signals are captured and the high voltage equipment that is required to do this. The fundamental principles behind the operation of this protection technique are also described.

The computer simulation of the power system is presented in Chapter 4. The primary arc model used is detailed and the modelling of the EHV transmission lines is described along with the configurations of the power sources.

Chapter 5 describes the individual components that make up the protection system and their implementation. This includes modal mixing, signal limiting, analogue to digital conversion, background noise considerations, digital filtering, signal enhancement and the decision logic that is used.

Teed circuit results are presented in Chapter 6. The networks used are described along with some typical results for internal and external faults. The scheme's performance for different fault types and positions is evaluated. Its

effectiveness is also examined for feed around paths, high resistance faults and alternative operating conditions. In addition, double circuit performance and sensitivity to line trap and stack tuner parameter variations are assessed.

Chapter 7 investigates the composite circuit problem. Underground cable modelling is discussed and the differences between the protection systems for the teed circuit and the composite circuit cases are highlighted. The composite networks used and some representative results are then presented.

Chapter 8 summarises the work covered in this thesis and draws the conclusions about it. Some suggestions for further work are also discussed.

Chapter 9 contains the references cited in this thesis. They are numbered in the order that they appear in the text and are listed by author, paper title, journal and date of publication.

The Appendix contains papers that have been, or will be, published by the author on the work that is contained within this thesis.

CHAPTER 2

POWER SYSTEM PROTECTION

2.1 Background

As power systems are pushed closer to their operating limits, the performance of the protection equipment becomes even more important. The potential damage to the expensive power system apparatus is increased, along with the disruption to consumers, if things go wrong. This risk can be reduced by using more advanced protection techniques. Very fast fault clearing times are important in maintaining power system stability, particularly when large amounts of power are transmitted between strong power systems on relatively weak interties [1]. However, speed must not be achieved through a loss of accuracy. The two important words in protection are *dependability*, the degree of certainty that a relay system will operate correctly, and *security*, the degree of certainty that a relay system will not operate incorrectly.

Over the last two decades there has been much activity in the protection of power systems [2, 3]. The electromechanical relays that have been used to protect transmission lines are slowly being replaced by microprocessor based relays [4]. Initially, the microprocessor relays implemented existing techniques electronically [5].

As their processing power has increased, the protection algorithms have become more sophisticated [6]. The techniques are enabling faster and more reliable schemes to be implemented and more complicated network configurations to be protected.

2.2 Conventional Protection

Most conventional protection schemes for extra high voltage (EHV) transmission systems, rely on extracting voltage and current signals around the power system frequency to detect faults [7, 8]. *Unit* protection schemes, such as *Current Differential* protection, discriminate between internal and external faults by using information from all of the line ends [9]. These relays are based on Kirchhoff's first law. When there is no fault, or a fault outside the protected circuit, the amount of current flowing into the circuit is equal to the current flowing out of the circuit. For an internal fault, the difference between the current flowing into the circuit and the current flowing out of the circuit is equal to the fault current. To avoid relay maloperation, this *differential* current must be above a *restraining* current. This is to compensate for errors due to differences in the current transformers which are magnified by the through current, for example.

The local phase currents are measured at each end and are then transmitted to the other relays. Each relay then calculates the differential and restraining currents for each phase and then, if necessary, sends a trip signal to its local circuit breaker. The transmission of the phase currents between terminals and the subsequent error

checking and synchronisation data, results in a large bandwidth medium being required. Fibre optic links are frequently used as they are capable of sending the large amounts of information quickly over the distances involved in transmission line protection. However, these types of communication links are expensive and the protection schemes can lose integrity if a channel fails [10].

Non-unit schemes use only locally derived information to detect faults and distance relays are the most common type. These use the instantaneous current and voltage signals to calculate an impedance value [11]. This corresponds to a distance measurement because the power conductors have a fixed impedance per unit length. In simple terms, if the impedance seen by the relay is less than the line impedance, then an internal fault is indicated, and if it is greater, then there is no fault. In practice, the problem is more complicated. The impedance seen by the relay is influenced by factors such as the load current, the fault impedance and any current infeeds.

Many of the relay trip characteristics form a circle in the impedance plane, the most common being the *Mho impedance characteristic.* A typical example is shown in Fig. 2.1. The diameter of the circle corresponds to the impedance setting (or *reach*, Z_L) and it is rotated according to the line impedance angle, θ. If the measured impedance falls within the boundary of the circle, a trip decision is issued.

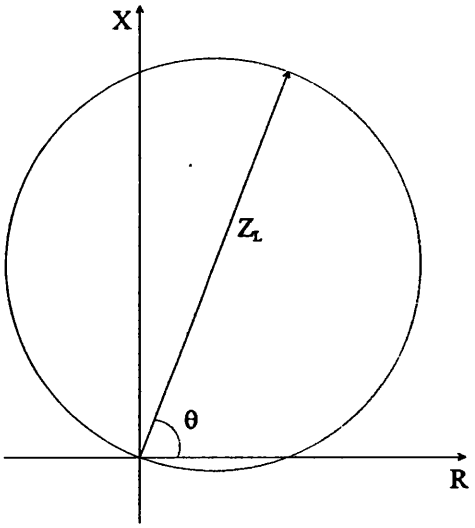


Fig. 2.1 - Mho characteristic

The reach of a distance relay cannot be set to the length of the line because of the inaccuracies of the impedance measurement. Therefore, the relay typically has three time graded zones: zone one covers 80% of the protected line; zone two covers 150% the protected line; and zone three covers 225% of the protected line, and 10% behind the line. Typically, zone one operates instantaneously, zone two operates after about a 0.3 s delay and zone three is delayed by approximately 0.5 s. [12]. A major advantage of the non-unit based schemes is that inherent backup results from the overlapping of the protection zones. However, power swing blocking may also be required to maintain the stability of the protection.

Digital distance protection schemes allow much more complicated trip criteria to be established. The trip characteristics are normally made up from a number of straight lines forming a quadrilateral, rather than being based on a circle. However, they do not overcome the problems with boundary accuracy and setting the reach points, particularly with complex power networks [13].

To improve the performance of distance schemes, a signalling channel is often connected between the line ends. The channel could be a high or low bandwidth medium, depending upon the complexity and cost of the system. There are many different signalling arrangements that can be used and this will depend on the circuit to be protected. However, they can be divided into two basic categories; *transfer trip schemes* where one relay initiates tripping of the remote circuit breakers and *blocking schemes* where tripping is inhibited [14].

Using non-unit protection devices with communication links has started to blur the boundaries between unit and non-unit protection schemes. The protection technique described in this thesis also sits in the grey area between the two categories. Essentially, it is a non-unit protection scheme as it relies only on locally derived information. However, it only protects a predefined zone, providing no backup protection, and it inherently restrains for faults outside that zone. Therefore, it also has the characteristics normally associated with unit protection.

2.3 New Types of Protection

2.3.1 Travelling Wave Protection

There has been increasing interest in *travelling wave* type protection methods [15, 16]. This has been largely confined to two terminal EHV lines and little has been reported on their application to more complicated networks, such as teed feeders. These techniques are based on the transmission line wave equation [17]. If the losses

are negligible and a distributed parameter model is used then:

$$\frac{\partial V}{\partial x} = -L\frac{\partial I}{\partial x} \tag{2.1}$$

$$\frac{\partial I}{\partial x} = -C\frac{\partial V}{\partial x} \tag{2.2}$$

where V is the phase voltage vector, I is the phase current vector, x is distance, L is the series inductance per unit length and C is the shunt capacitance per unit length. These have the well known solution found by D'Alembert:

$$V(x,t) = \frac{1}{2}[f_1(t-\alpha x) + f_2(t+\alpha x)] \tag{2.3}$$

$$I(x,t) = \frac{1}{2Z_0}[f_1(t-\alpha x) - f_2(t+\alpha x)] \tag{2.4}$$

where $\frac{1}{\alpha} = \frac{1}{\sqrt{LC}} =$ surge velocity, (2.5)

and $Z_0 = \sqrt{\frac{L}{C}} =$ line characteristic impedance. (2.6)

$f_1(t, x)$ and $f_2(t, x)$ are the forward and backward travelling wave functions that are set up by the fault and are defined by the boundary conditions. The travelling waves propagate throughout the network at just below the velocity of light and are partly, or fully, reflected by impedance discontinuities, such as the line terminations and the fault point. Processing of the initial waves set up by the fault and their subsequent reflections enable a trip decision to be made [18].

2.3.2 Non-power Frequency Component Protection

Work has also been done on using non-power frequency components for protection purposes. These exploit the wideband noise signals that are emitted by arcing faults. The detection of low level faults on low voltage distribution feeders has been investigated using these non-power frequency current components over a number of years [19, 20, 21].

The monitoring of high frequency current components (typically 100 kHz) with a special wideband current transducer was suggested by Mehdi [22]. Johns and Agrawal [23] proposed capturing the high frequency components of the system voltage by using a tuned circuit with a conventional capacitor voltage transformer. A directional detector was used to distinguish between forward and reverse faults. The principles of this technique have been developed to produce a discriminative non-unit protection scheme for plain EHV transmission lines [24]. This work expands this technique further to protect more complicated networks.

2.4 Complex Circuit Arrangements

2.4.1 Teed Circuits

The high cost of purchasing and installing new equipment and constructing new transmission lines has encouraged planners to examine new and more cost effective ways of reinforcing power systems. Increasing environmental pressures have also made it harder to obtain the necessary consents for new overhead line routes. Therefore, more complicated network configurations have been developed to overcome these restrictions.

Converting existing under-used plain feeders into teed circuits is one such solution and it has several financial benefits. Typically, it will require a shorter length of new line to be constructed and expensive high voltage apparatus, such as circuit breakers, current transformers (CTs) and voltage transformers (VTs), will only be required at the new terminal. This can be illustrated by using the simple network shown in Fig. 2.2.

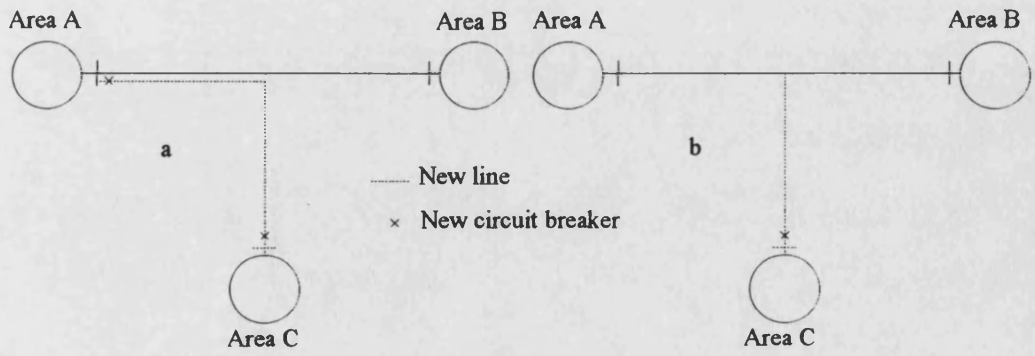


Fig. 2.2 - Teed circuit advantages

An existing transmission line connects area A to area B, and area C requires a new infeed. The first option (Fig. 2.2a) is to build a new line between A and C, so auxiliary equipment, circuit breakers, CTs and VTs etc, will be needed at both ends on all three phases. Turning the existing line into a teed circuit, however, will need a shorter length of new line and new equipment only at end C (Fig. 2.2b).

Protecting teed circuits can be difficult using conventional techniques, particularly using non-unit principles [25, 26]. Variations in the system operating conditions can cause serious problems in setting the reach of the widely used distance relays [27]. Factors such as the amount of infeed to the tee point from the third terminal, and the source configuration, have a serious effect on the impedance seen by the distance relays. For protection relays based on travelling waves, the reflection from the tee point impedance discontinuity, coupled with those from the line terminations and fault point, can severely affect the voltage and current waveforms detected at the line ends [28]. Many of these problems are compounded if the distances from the ends of the transmission line to the tee point are significantly different.

A large number of schemes have been proposed to overcome the problems of protecting teed transmission circuits. One method is to install extra voltage and current transducers, and relays, at the tee point [29]. The extra measurement point allows the tee to be treated as a shorter plain section of line. High performance communication equipment is also required to provide the necessary blocking or transfer trip signals. The disadvantage of this type of scheme is that expensive relaying equipment and

instrument transformers at the tee point are needed in addition to the communication links. Also, it may not have large cost savings as the measurement equipment would have to be installed at the tee point, which is most likely to be in an exposed area, rather than in a substation at the line end.

Current differential relaying techniques have been used extensively to protect teed circuits. These rely on the same basic principle as the two-terminal case with each end requiring the current information from the other two ends. The communication overhead is, therefore, increased along with the amount of calculations, and again wideband communication equipment is normally required. Fibre-optic cables are often used [30] as well as microwave links [31]. These schemes require the data from each of the line ends to be time-tagged or synchronised, so that the data can be correctly time aligned.

Operating conditions can also reduce the performance of the protective devices. High through load currents can cause false trips on current differential schemes. The large current highlights any slight difference in the CT ratios and the resulting signal may exceed the bias signal and give an incorrect trip decision. In practice, the teed circuit may also have to be operated with one or two of the line ends open circuited. This mode of operation will frequently mean the protection scheme will have to be altered to cope with the new configuration.

2.4.1.1 Feed around paths

Under certain circumstances, an internal fault may appear to be external to current differential schemes. If there is an additional connection between two of the terminals forming the tee, then a fault occurring close to one of these terminals can set up the current flow shown in Fig. 2.3.

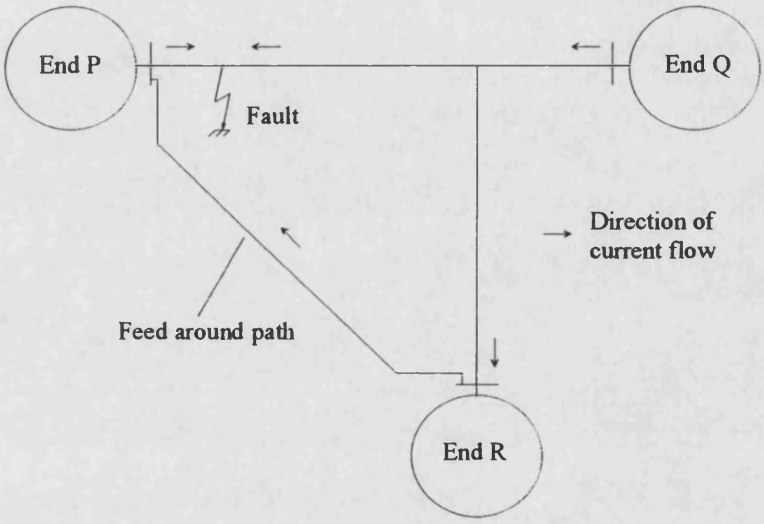


Fig. 2.3 - Feed around path current flow

The currents at ends P and Q flow into the protected circuit as expected, but at end R, the current flows out of the network. This can then initiate a blocking signal which prevents the protection from operating. This situation occurs if the source at R is significantly weaker than the source at Q. Therefore, current is supplied to the fault from Q via end R and through the so called *feed around path*. These paths are very likely to be present in a highly connected transmission network such as the British supergrid system. More recent protection techniques have used relaying signals formed

from a combination of sampled current and voltage signals to overcome this problem [32].

2.4.2 Composite Circuits

Many transmission networks contain circuits which consist of overhead lines and underground cable sections. These *composite circuits* can also be difficult to protect because of the large differences in the properties of overhead lines and underground cables. Distance protection relays can have problems because the underground cables have a much higher impedance per unit length and their sequence impedances are significantly different [33].

Compared with overhead lines, cables have a large shunt capacitance, much slower propagation velocities and a much greater attenuation rate [34]. This is because the cables consist of a central phase conductor which is surrounded by a conducting sheath and a metallic armour. These are separated by insulating layers of oil impregnated paper or polyethylene. This causes the cables to have six modes of propagation, instead of the three modes found with overhead lines. The three additional modes are associated with the sheaths of the single phase cables.

Underground cables are frequently found on EHV transmission systems for many reasons. It may be the most practical way for the circuit to enter a substation because of the number of existing overhead lines limiting the amount of available

space. The circuit may be passing through an environmentally sensitive area and so the circuit may be placed underground because of this.

Many papers have described different methods of modelling underground cable networks [35, 36], but little has been published on protecting them. Generally, they are protected using standard plain transmission line techniques with modified settings. These include distance protection and current differential protection.

CHAPTER 3

SIGNAL DETECTION AND OPERATION

3.1 Signal Detection

Sudden changes in the power system voltage, due to arcing faults and travelling waves, create wideband high frequency (HF) signals on the associated EHV power lines [37, 38]. These HF signals can be used for protection purposes [39], but they are generally outside the bandwidth of most conventional voltage transducers. Studies [40, 41] have shown that the HF signals of interest can be detected with equipment that is normally used for power line carrier (PLC) communication [42]. A stack tuner is used to capture the relevant signals while a PLC signal line trap confines them to the protected zone and gives the technique its discriminative properties. This arrangement is shown in Fig. 3.1 and is connected to all three phases at each end of the line to be protected. Typically, coupling equipment is only fitted to two phases in PLC protection schemes and so an additional line trap and stack tuner would have to be fitted to the third phase for it to be converted for use with this fault generated noise protection scheme.

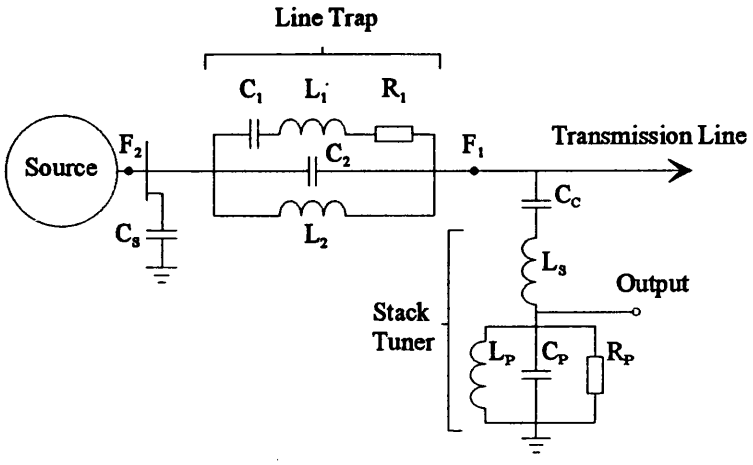


Fig. 3.1 - Line trap and stack tuner arrangement

The stack tuner is connected to the coupling capacitor, C_c, of a standard capacitor voltage transformer (CVT) and is designed to capture a narrow band of high frequencies around a specified centre frequency. It therefore offers a very high impedance at the power frequency and has an impedance very close to the line characteristic impedance at the tuned centre frequency. This minimises the attenuation at the tee point [43] and correctly terminates the line.

The line trap is the standard wideband type used for PLC applications by the National Grid Company (NGC) in Britain. It is tuned to block a narrow band of high frequencies by exhibiting a high impedance around a specified centre frequency while offering a low impedance at all other frequencies. The line trap series resistance, R_1 is increased to approximately ten times the line characteristic impedance to increase the attenuation of the line trap and so give better discrimination between internal and external faults.

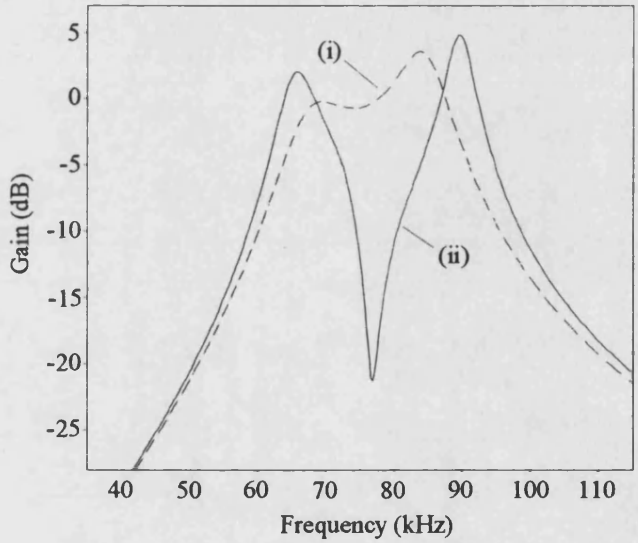
The most suitable frequency band for the protection scheme has been investigated in a number of studies [44, 45]. Practical considerations play a significant role in the choice of the centre frequency, as this affects the sampling frequency required and therefore the time in which all of the relay's calculations have to be completed. With currently available microprocessor hardware, it was determined that 5 μs would be sufficient time to carry out the necessary protection calculations and so a sampling rate of 200 kHz was chosen. According to the Nyquist sampling theorem, the highest frequency that can therefore be detected is 100 kHz. NGC PLC Communication Band 1 was chosen as it corresponds to a frequency band of 70 to 81 kHz with a centre frequency of 75 kHz. The line trap and stack tuner parameters for this band are shown in Table 3.1.

Table 3.1 - Line trap and stack tuner parameters

Parameter	Value	Parameter	Value
R_1	2700 Ω	C_c	2 nF
L_1	3.97 mH	L_s	2.10 mH
C_1	1.12 nF	R_p	270 Ω
L_2	185 μH	L_p	133 μH
C_2	24.8 nF	C_p	35.3 nF

The stray shunt capacitance of the substation busbars is represented by C_s in Fig. 3.1 and a typical value of 0.1 μF was used in the simulations. This strengthens the barrier between internal and external faults as it provides a low impedance path to ground for the high frequencies blocked by the line trap.

The frequency response of the line trap and stack tuner arrangement for inputs in front of the line trap, F_1 (in Fig. 3.1), and behind the line trap, F_2, can be seen in Fig. 3.2.



(i) Input in front of line trap (internal)
(ii) Input behind line trap (external)

Fig. 3.2 - Line trap and stack tuner frequency response

For a disturbance in front of the line trap, F_1, there is very little attenuation across the tuned band and increasing attenuation on either side. This is in contrast to

a disturbance just behind the line trap at F_2. Here, the bandstop nature of the line trap is demonstrated by the 20 dB attenuation of a narrow band of frequencies around the centre frequency of 75 kHz. It is this blocking action that enables external faults to be discriminated from internal ones.

3.2 Fundamental Operating Principle

The basic concept of this protection technique can be best understood by examining some typical single phase to earth fault output waveforms. A symmetrical tee network with 80 km tee leg lengths and 20 GVA source capacities is used for this explanation. For an internal fault occurring at a voltage zero at F_1 in Fig. 3.1 and an external fault at F_2, the time domain outputs from the stack tuner closest to the fault are shown in Fig. 3.3.

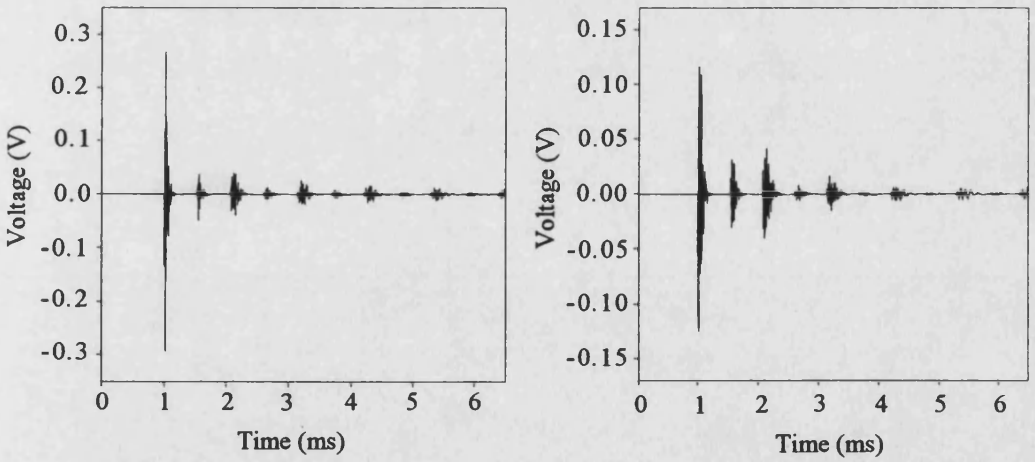
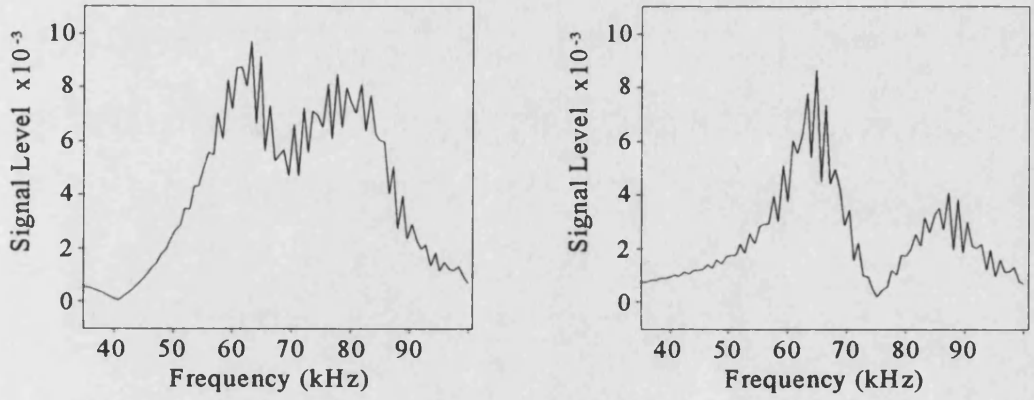


Fig. 3.3 - Internal and external fault time domain outputs

In the time domain, both the internal and external fault responses show the characteristic noise bursts associated with this technique. The initial burst is due to the electric arc at fault inception and the subsequent bursts are due to reflections from the tee point and the remote terminals. In this form, it is very difficult to detect any fundamental differences between the two waveforms, except slight variations in the signal magnitudes. However, in the frequency domain, the severe attenuation caused by the line trap in the external fault case is clearly visible (Fig. 3.4).



a Internal Fault Frequency Spectrum

b External Fault Frequency Spectrum

Fig. 3.4 - Internal and external fault frequency spectra

This significant difference in the frequency spectra of the signals makes it possible to discriminate between internal and external faults. This is achieved by extracting components proportional to the spectral power at the centre frequency, 75 kHz, and at a slightly lower reference frequency. These are known as the *operate* and *restraint* quantities respectively. The operate quantity is divided by the restraint quantity to form a *discrimination ratio*. For an internal fault, this ratio will be approximately equal to or greater than unity, as the operate and restraint quantities are

comparable. For an external fault, however, the operate quantity will be substantially less than the restraint quantity and so the ratio will approach zero. The ratio activates a counting algorithm which issues a trip decision when the counter's value exceeds a predetermined threshold level. This will be described in greater detail in section 5.6.

CHAPTER 4

POWER SYSTEM SIMULATION

The fault data used to develop the protection algorithm was generated using the well proven Electromagnetic Transients Program, EMTP [46]. This contains mathematical models of the power system components allowing the behaviour of different network configurations to be studied under various fault conditions. The data was calculated at 1 μs intervals (ie simulated at 1 MHz) to give improved accuracy. Every fifth data value was then used to give the desired sampling rate of 200 kHz.

4.1 Primary Arc Model

To produce accurate fault data, an electric arc model was included in the simulations. The Transient Analysis of Control Systems (TACS) subsection of the EMTP was used to do this. It allows calculations which model the arc behaviour to be done between each time step and the new information can then be used to solve the electrical network at the next time step.

Following a fault on a transmission line, an electric arc develops which is frequently across the line insulator string. The primary arc exists from the time of fault inception to when the circuit breakers open. This then becomes a secondary arc once the circuit breakers have opened, isolating the line. This work is only concerned with what happens during the primary arcing period.

The fault arc path is commonly modelled as an ideal short circuit or a low value resistance [47]. Work has also been done on more accurate piecewise arc characteristics [48]. However, the non linear behaviour of the primary arc is fundamental to this work, so a time-varying arc resistance method was used. This model is based on the energy balance in the arc column developed by Hochrainer [49]. Control system and switching arc theories have been applied to this to describe the dynamic behaviour of the arc [50] and it can be represented by:

$$\frac{dg}{dt} = \frac{1}{\tau}(G-g) \tag{4.1}$$

where g is the time varying arc conductance, G is the stationary arc conductance and τ is a time constant. The stationary arc conductance, G can be physically interpreted as the arc conductance value that would set in if the current were maintained under constant external conditions for a sufficiently long time and can be evaluated from:

$$G = \frac{I_M}{(V_o + R I_M)\ell} \tag{4.2}$$

where I_M is the arc current magnitude, V_o is the constant voltage parameter per unit

arc length, R is the resistive component per unit arc length and ℓ is the time dependant arc length. The parameter values have been determined from the experimental data discussed in reference [50].

The time varying arc conductance is calculated by solving the arc equation (Equ. 4.1) at each time step using Equ. 4.3 by making the assumption that the stationary arc conductance and time constant remain constant during each time step.

$$g(t) = G(t-\Delta t) - [G(t-\Delta t) - g(t-\Delta t)]\exp\left(\frac{-\Delta t}{\tau}\right) \qquad (4.3)$$

The reciprocal of this then gives the time varying arc resistance which is used to represent the arc in the simulation. Some waveforms from a typical arcing fault using this model are shown in Fig. 4.1.

The distortion of the voltage waveform by the non linear nature of the arc can clearly be seen in Fig. 4.1a. The first five milliseconds show the power system voltage before the fault is applied. The distortion in the post-fault voltage occurs twice per 50 Hz cycle and this is due to the arc restriking as it passes through a current zero (Fig. 4.1b). The time of the restrike will therefore depend on the amount of dc offset on the current waveform and this is strongly influenced by the fault inception angle. In this case, the restrike occurs every 10 ms as there is no dc offset associated with this voltage maximum fault. Additional HF signals are also generated with every restrike giving the protection technique further opportunities to correctly identify the fault. The resulting arc cyclogram can be seen in Fig. 4.1c.

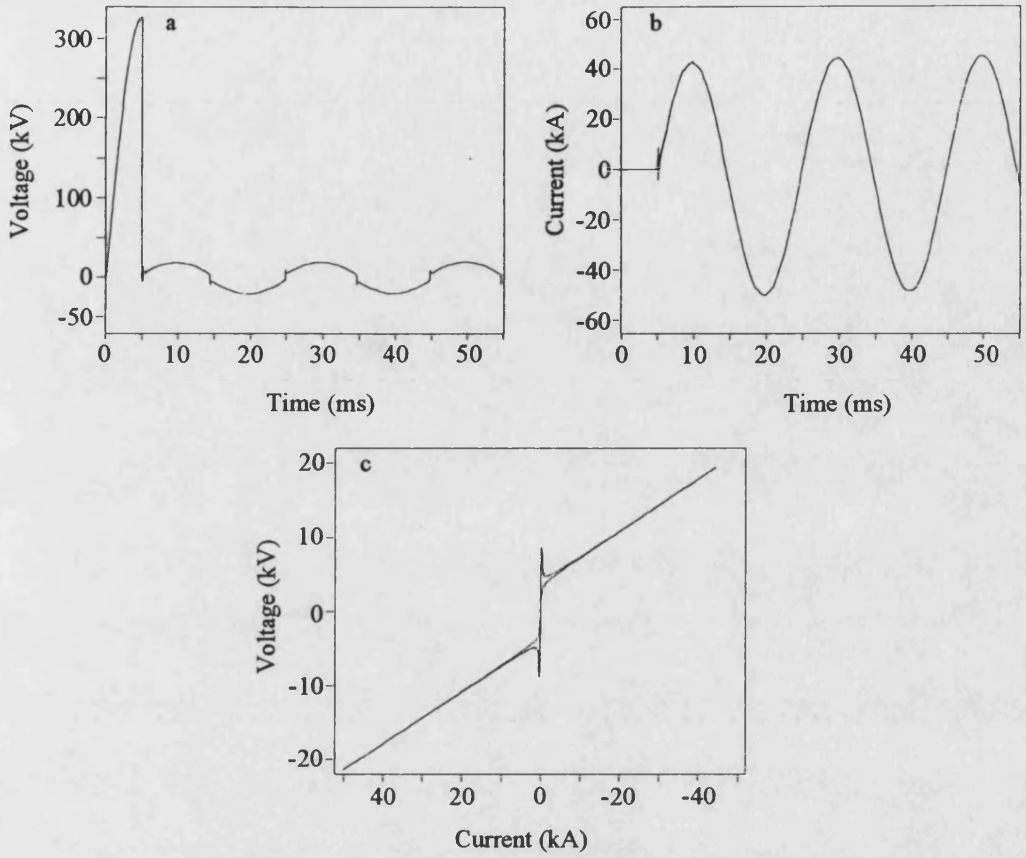


Fig. 4.1 - Non linear arc behaviour

4.2 Transmission Lines

The transmission lines modelled, were based on a single circuit of a typical quad-conductor 400 kV vertical construction overhead line of the type currently used on the British supergrid system [51]. The phase conductors are 4 x 54/7/0.33 cm Aluminium Conductor Steel Reinforced (ACSR) with 0.305 m bundle spacing and the earth wire is 54/7/0.33 cm ACSR. The positioning of the line conductors is shown in Fig. 4.2.

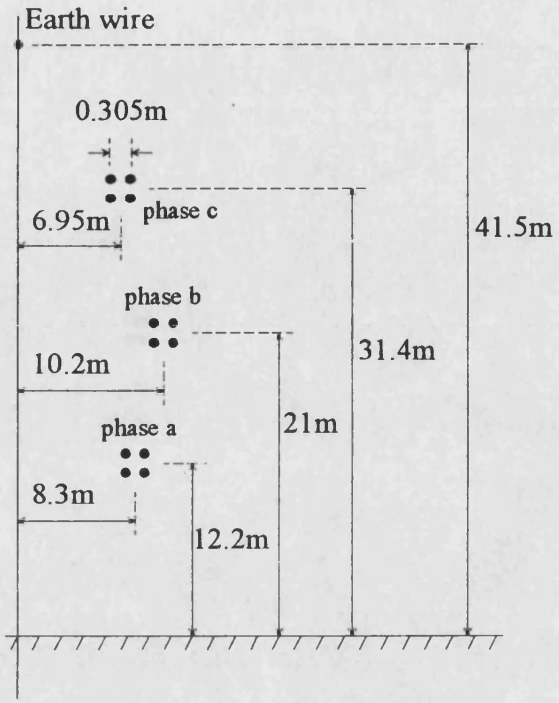


Fig. 4.2 - 400 kV Overhead line

The British supergrid network is highly interconnected and the line lengths are relatively short. Therefore, the transmission lines are not transposed and this is reflected in the modelling. The frequency dependence of the line parameters were taken into account using the fitting algorithm developed by J. R. Marti for the EMTP [52]. The earth resistivity was taken to be 100 Ωm and a nominal power system frequency of 50 Hz was used.

4.3 Source Modelling

Each phase of the power system source was modelled as a voltage source in series with a lumped resistance and inductance to represent the short circuit capacity of the terminating busbar. The neutrals of the three phases were all solidly grounded to give a zero phase sequence to positive phase sequence ratio (Z_{s0} : Z_{s1}) of unity. A source X : R ratio of 30 was assumed throughout the studies and was calculated as follows:

$$Z_s = \frac{V_L^2}{SVA} \tag{4.4}$$

where Z_s is the source impedance (Ω), V_L is the operating line voltage (V) and SVA is the source short circuit level (VA).

The source resistance, R_s (Ω) and source reactance, X_s (Ω) can then be calculated from:

$$Z_s = R_s + jX_s \tag{4.5}$$

$$X_s = Z_s.\sin\left(\tan^{-1}(X{:}R\ ratio)\right) \tag{4.6}$$

$$R_s = \frac{X_s}{X{:}R\ ratio} \tag{4.7}$$

CHAPTER 5

PROTECTION SYSTEM

The full protection system consists of a number of functional units. These are shown in Fig. 5.1. All of the operations are performed on the measured signals at each end of the circuit to give the locally derived trip decisions. The operate and restraint quantities are calculated for both of the modes and so two discrimination ratios are calculated at each end.

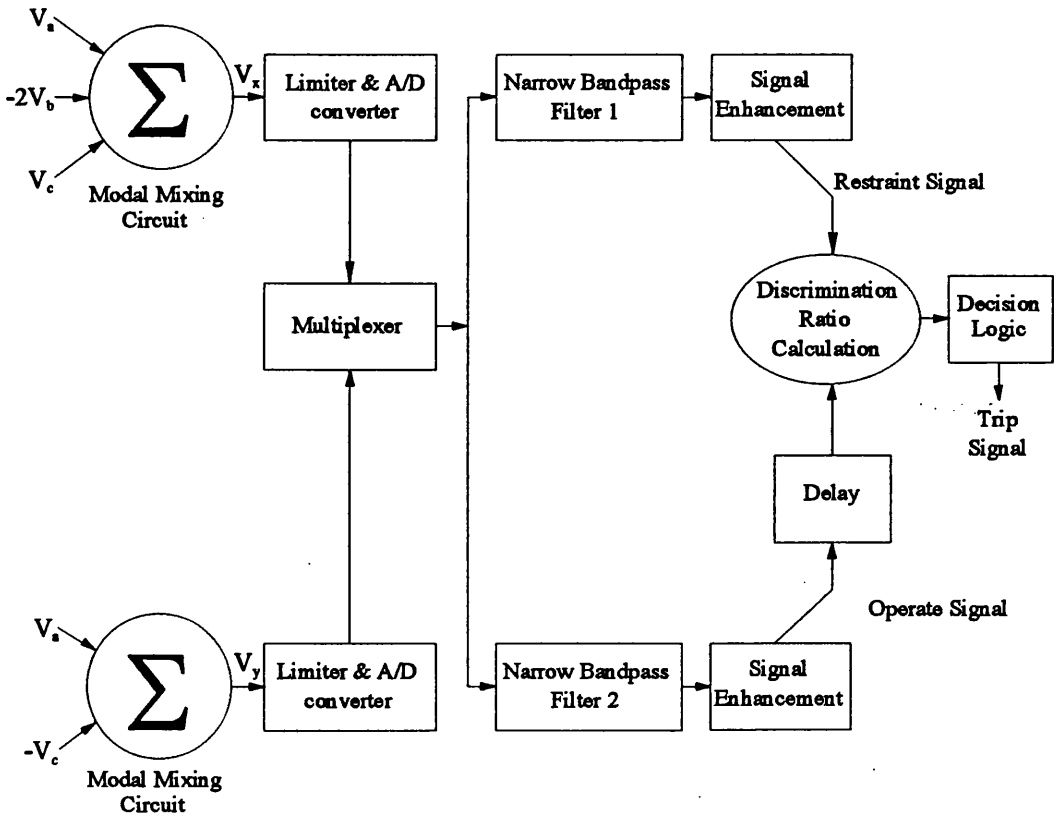


Fig. 5.1 - Protection system block diagram

5.1 Modal Mixing Circuit

As this technique relies on high frequency signals which propagate along the power conductors, it is susceptible to extraneous signals being induced onto the line from adjacent power conductors, or communication circuits, for example. These interference signals are predominantly associated with the earth (or common) mode and could threaten the stability of the relay. This problem can be avoided by using modal components which allows the phase voltages to be transformed into three independent modes [53]. These are the earth (or common) mode and two aerial modes. Their derivation is shown below.

A distributed parameter three phase transmission line can be described by the following differential equations:

$$\frac{dV}{dx} = -ZI \quad ; \quad \frac{dI}{dx} = -YV \tag{5.1}$$

where

$$V = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad ; \quad I = \begin{bmatrix} I_a \\ I_b \\ I_c \end{bmatrix} \tag{5.2}$$

Z is the impedance matrix and Y is the admittance matrix.

$$\frac{d^2V}{dx^2} = -Z\frac{dI}{dx} = ZYV = PV \tag{5.3}$$

and similarly

$$\frac{d^2I}{dx^2} = YZI = P^TI \tag{5.4}$$

These equations cannot be solved directly so a *Modal* transformation is introduced as follows:

$$Let \quad V = SV^c \tag{5.5}$$

$$\therefore \frac{d^2}{dx^2}(SV^c) = PV = PSV^c \tag{5.6}$$

$$\frac{d^2V^c}{dx^2} = S^{-1}PSV^c \tag{5.7}$$

$S^{-1}PS$ is arranged to be diagonal and so S is a matrix of Eigenvectors of P. These modal components are, therefore, independent of other components and the Eigenvalues of P are the *Modal propagation constants*. The components of V^c are associated with the *natural modes of wave propagation* and S is the *Modal voltage matrix*.

For currents

$$Let \quad I = QI^c \tag{5.8}$$

$$\therefore \frac{d^2 I^c}{dx^2} = Q^{-1} P^T Q I^c \tag{5.9}$$

Again, $Q^{-1}P^TQ$ is arranged to be diagonal and Q is the *Modal current matrix*. There are a number of different transformation matrices, but the most common is the *Clark's* transformation. This assumes ideal line transposition and is suited to a majority of practical applications and is given by Equ. 5.10.

$$S = Q = \begin{bmatrix} 1 & 1 & 1 \\ 1 & 0 & -2 \\ 1 & -1 & 1 \end{bmatrix} \tag{5.10}$$

But

$$V^c = S^{-1} V \tag{5.11}$$

$$\therefore \begin{bmatrix} V^{c1} \\ V^{c2} \\ V^{c3} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ \frac{3}{2} & 0 & -\frac{3}{2} \\ \frac{1}{2} & -1 & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{5.12}$$

The behaviour of any uniform line can be divided into a number of independent modes of propagation. In general $Q \neq S$, so the voltage and current distribution in the same mode will be different. Only the voltages are of interest in this work and so any changes to the modal current distribution caused by the amount of line transposition for example, are not of any interest.

Only the two aerial modes are required and they can be simplified to:

$$V_x = V^{c2'} = V_a - V_c \tag{5.13}$$

and

$$V_y = V^{c3'} = V_a - 2V_b + V_c \qquad (5.14)$$

where V_x, V_y, $V^{c2'}$ and $V^{c3'}$ are the aerial mode voltages and V_a, V_b and V_c are the phase voltages. The two aerial modes are able to detect all types of line faults and as the earth mode signal is not used, the potential problems due to mutual coupling with other circuits and interference sources are alleviated.

5.2 Signal Limiting and Analogue to Digital Conversion

The two modal signals have a very large dynamic range. For example, for faults occurring near voltage maximum, there is a very large initial burst of HF signals of several kilovolts which is mainly due to the significant travelling wave components that are associated with such faults. Therefore, the bursts of HF signals created by the non linear nature of the fault arc current get swamped by the travelling wave components, at least during the very short time following fault inception. Conversely for faults near voltage zero, hardly any travelling waves are generated and the HF signal bursts are predominantly due to the non linear arcing fault. These signals normally only have a magnitude of several volts.

If the analogue to digital (A/D) conversion process were to handle the complete range of signal levels, a resolution of more than 16 bits would be required. However, it is not practical (nor economical) to handle this degree of precision in a protective relay and the most common A/D converter used has a 12 bit resolution. Therefore, to retain relay sensitivity to the majority of practically encountered faults, including low signal level faults, the dynamic range of the relay has to be reduced. This is

achieved by passing the analogue HF signals through a signal limiter to clip them to the required level.

A direct consequence of clipping is that for faults with very large initial bursts, there is some signal corruption and a reduction in the spectral power. The clipping level and the auxiliary step down transformer connected to the stack tuner output has to be carefully chosen to ensure that the minimum expected fault signals are well above the background noise levels (which are discussed in section 5.3). In practice, the auxiliary transformer is a specially designed wideband device which has a radio-metal core and a turns ratio of 200 : 1. It will be shown in section 6.4 that the clipping of high level signals does not adversely affect the performance of the relay and the required dynamic range is adequately covered.

The phase signals from the stack tuners' auxiliary transformers are therefore limited to ± 10 V directly after being combined to form the two modal signals. The signals are then passed through a fourth order Butterworth anti-aliasing filter with a cutoff frequency of 100 kHz before being inputted into the A/D converter. The filter is implemented as two second order sections, each having the transfer function :

$$T(s) = \frac{2.04931 \times 10^{11}}{s^2 + 452693.53\, s + 2.04931 \times 10^{11}} \qquad (5.15)$$

All of the analogue operations, such as the signal limiting, modal mixing and anti-alias filtering, were performed within the EMTP simulations.

5.3 Background Noise Considerations

In practice, there is spurious HF noise present on the power system. This can be due to corona discharge, the thermal agitation of conductors or electromagnetic interference for example. High voltage laboratory tests [54] and practical experience has shown that the maximum level of background noise likely to be admitted into the front end of the relay is less than 40 mV. This corresponds to eight quantum levels based on the ± 10 V, 12 bit A/D converter. A threshold set at this level within the relay software thus ensures that the relay is stable under healthy conditions, without its sensitivity being unduly affected for internal faults.

5.4 Digital Filtering

The relevant high frequency components of the modal input signals are extracted with two digital narrow bandpass filters. Sixth order elliptic infinite impulse response (IIR) filters are used as they give a very rapid transition between the stop and pass bands. This enables the filters to be constructed with very low filter orders and so minimise their group delays [55]. The choice of the filter centre frequencies is crucial to the correct operation of this protection scheme. The *operate* filter frequency is fixed by the centre frequency of the line trap, in this case 75 kHz. The *restraint* filter frequency is chosen to give the best ratio for discrimination purposes. A large number of computer aided design (CAD) studies were carried out to achieve the optimum results. For the teed circuit case, the best results were obtained using a

2 kHz bandwidth filter at the operate frequency of 75 kHz and a 1 kHz bandwidth filter at a restraint frequency of 63 kHz. The Z domain filter transfer functions are of the form shown in Equ. 5.16 and their frequency responses are shown in Fig. 5.2.

$$H(z) = G_0 \frac{(a_0 + a_1 z^{-1} + a_2 z^{-2})(a_3 + a_4 z^{-1} + a_5 z^{-2})(a_6 + a_7 z^{-1} + a_8 z^{-2})}{(b_0 + b_1 z^{-1} + b_2 z^{-2})(b_3 + b_4 z^{-1} + b_5 z^{-2})(b_6 + b_7 z^{-1} + b_8 z^{-2})} \quad (5.16)$$

where a_n and b_n are the individual filter coefficients and these are shown in Tables 5.1 and 5.2.

Table 5.1 - Restraint filter coefficients

G_0		0.0012918748	
a_0	1	b_0	1
a_1	0	b_1	0.72761291
a_2	-1	b_2	0.97629619
a_3	1	b_3	1
a_4	0.63465118	b_4	0.70084357
a_5	1	b_5	0.98931271
a_6	1	b_6	1
a_7	0.83380741	b_7	0.76360041
a_8	1	b_8	0.98945445

Table 5.2 - Operate filter coefficients

G_0		0.0049238537	
a_0	1	b_0	1
a_1	0	b_1	1.3846364
a_2	-1	b_2	0.95720547
a_3	1	b_3	1
a_4	1.3094460	b_4	1.3555679
a_5	1	b_5	0.98285133
a_6	1	b_6	1
a_7	1.5066711	b_7	1.4477929
a_8	1	b_8	0.98392612

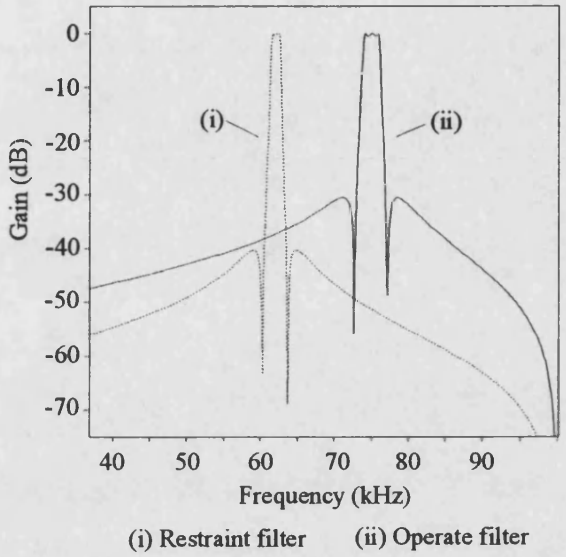


Fig. 5.2 - Digital filter frequency responses

Care has to be exercised when fixing the word length of the filter coefficients as any loss in their precision causes the filter pole positions to move slightly. This in turn may be sufficient to move the poles outside the Z domain unit circle, causing the filter to become unstable. It is thus vitally important to check this process very carefully. The risk of filter instability can be minimised by implementing the filters using cascaded second order sections [56].

5.5 Signal Enhancement

The power of each of the two frequency bands needs to be measured so that a comparison can be made. The mean power, P_m of a signal $x(t)$ can be measured using Equ. 5.17, where T is the time limit [57].

$$P_m = \frac{1}{T} \int_{-\frac{T}{2}}^{\frac{T}{2}} x^2(t)\, dt \tag{5.17}$$

The signals being dealt with are in the digital domain and so the integral is replaced with a summation. The filter outputs are first squared and then averaged over a 250 sample (1.25 ms) long moving window as shown in Equ. 5.18 to give a measure of their spectral power.

$$Y(n\Delta t) = \frac{\sum_{k=n-L_{av}}^{n} V_{fx}(k\Delta t)^2}{L_{av}} \tag{5.18}$$

where $Y(n\Delta t)$ is the enhanced output at time $n\Delta t$, n is the time step number, Δt is the time step (sampling interval), V_{fx} is the bandpass filter output and L_{av} is the length of moving average window (250 samples ≡ 1.25 ms at the 200 kHz sampling rate).

Because the two IIR filters have slightly different group delays, the operate signal has to be delayed by 40 samples to equalise them and so eliminate any phase shift errors. It is assumed that a high performance processor with floating point arithmetic would be used in the hardware implementation of the relay design. This removes the need to use scaling factors to avoid arithmetic overflow problems.

5.6 Decision Logic

The relay is able to distinguish between internal and external faults by calculating a *discrimination ratio*. This is calculated from the ratio of the enhanced operate filter output to the enhanced restraint filter output. For internal faults, this ratio will be approximately equal to or greater than one, whereas it will be very close to zero for external faults. In order to improve relay security, a counting regime was also incorporated into the relay algorithm for each of the modes. When either of the trip counters exceed a preset threshold level, an output to the line circuit breakers would be initiated.

Extensive CAD studies were carried out to ascertain the optimum settings of the counting regime and trip threshold level. This involved simulating a wide range of fault conditions and then calculating the filter responses and discrimination ratios. The decision logic was then applied to these results and the performance of different counting regimes and threshold levels was assessed. The counting regime that was decided upon is summarised in Table 5.3. A threshold level of 250 was found to give a relay trip in approximately one millisecond for internal faults, while the counter remained well below this level and restrained for external faults.

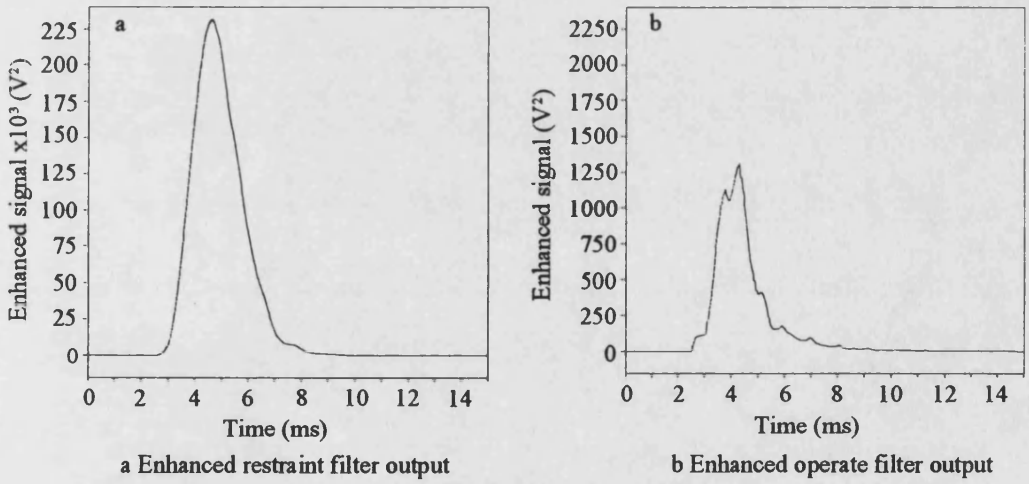
Table 5.3 - Counting regime

Discrimination Ratio, D_r	Counter Increment
$D_r \geq 0.8$	+ 10
$0.8 > D_r \geq 0.6$	+ 9
$0.6 > D_r \geq 0.5$	+ 4
$0.5 > D_r \geq 0.4$	+ 1
$0.4 > D_r \geq 0.1$	- 1
$0.1 > D_r \geq 0.005$	-3
$0.005 > D_r$	- 10

As can be seen from the table, when the discrimination ratio, D_r, is close to, or above one, the counter is incremented rapidly as the ratio gives a strong indication of an internal fault. When the ratio is between 0.6 and 0.4, the counter is incremented more slowly as there is some degree of uncertainty about the presence of an internal fault. The counter is decremented slowly, when the ratio falls below 0.4. The counter is decremented rapidly, when the ratio is close to zero as this gives a strong indication of an external fault, but its value is never allowed to fall below zero. Division by zero errors are avoided by not allowing the enhanced restraint output to fall below a minimum value of 0.02. The enhanced operate output is set to zero if it drops below the same value, forcing the discrimination ratio to zero.

5.6.1 Rising Ratio Algorithm

An additional algorithm has also been included to minimise one of the problems encountered during the CAD stage. Under certain conditions, an incorrect trip decision was given several milliseconds after the initial correct external fault classification. This was caused by the discrimination ratio reaching an erroneously high value. When the relay detects the HF components, the enhanced filter outputs rise to their peak values. These then decay at a rate determined by the length of the moving average window. This is shown in Fig. 5.3.



a Enhanced restraint filter output

b Enhanced operate filter output

Fault inception, $t_f = 2.5$ ms

Fig. 5.3 - Enhanced filter outputs

During the period of time shortly after the fault occurrence, the enhanced outputs are close to their maximum values and the correct trip decision is made for

both internal and external faults. However, as the HF signals reduce, the enhanced outputs start to decay towards zero. Initially this does not cause a problem, but as both outputs reduce, the discrimination ratio can start to rise and give an incorrect indication of an internal fault. This is clearly shown in Fig. 5.4.

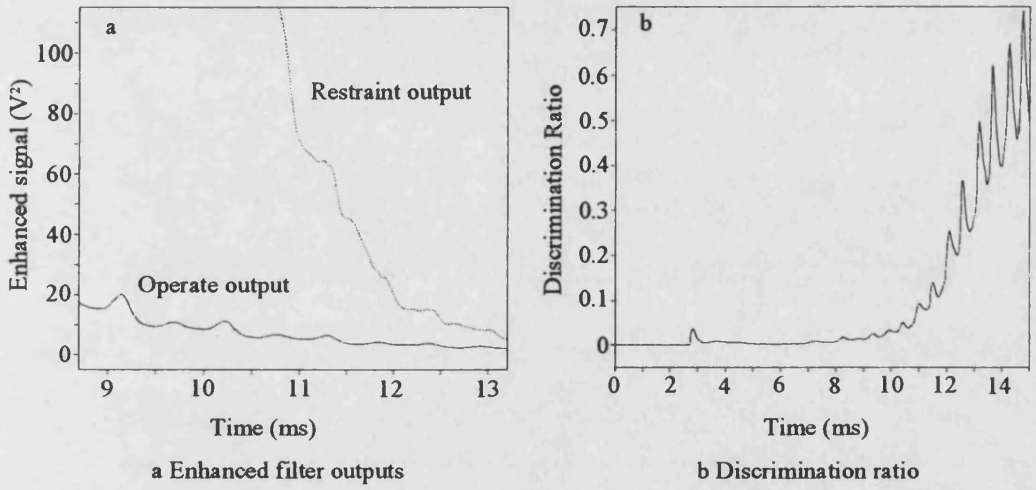


Fig. 5.4 - Rising ratio problem

This problem has little to do with the incoming signals, but is mainly due to the way they decay through the enhancement process. The additional algorithm solves this by initially monitoring the peak value of the enhanced operate output. When the output falls below one third of its maximum value, the rising ratio algorithm is started. A flow chart showing its operation is shown in Fig. 5.5.

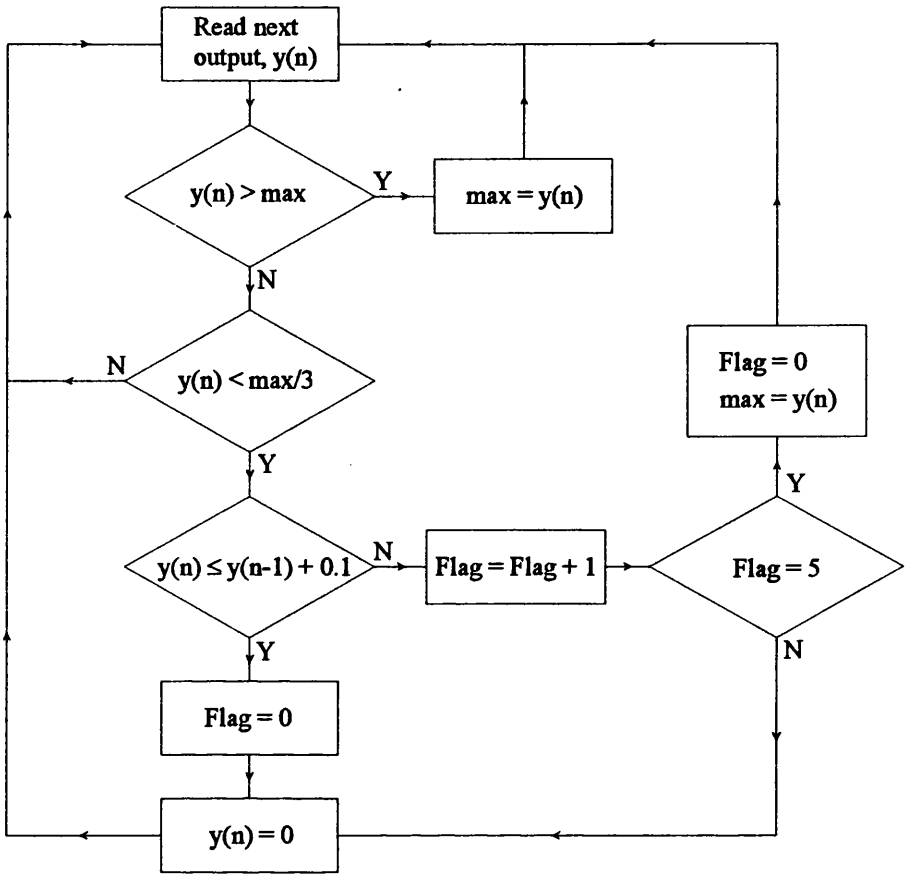


Fig. 5.5 - Rising ratio algorithm

If the current output is less than the last output plus a constant, ie still reducing, then the output is set to zero leading to a discrimination ratio of zero. If this does not happen for five consecutive values, ie the output is not dropping quickly enough or it is increasing, the current output is not altered and the peak monitor is set to this value. A constant value of 0.1 was found sufficient to eliminate the rising ratio problem without affecting the relay's sensitivity to subsequent bursts.

For the work presented in this thesis, all of the digital signal processing, ie the A/D conversion through to the trip output, has been implemented using off-line computer programs written in C. This means that no delays, due to the analogue processing and the finite amount of time the processor takes to perform the calculations, for example, are taken into account. It is envisaged that the relay calculations will be performed using four Texas Instruments TMS320C40 floating point parallel processors. These are specially designed for digital signal processing applications and are capable of performing 275 million operations per second. It is estimated that with this arrangement, the trip output would still be given less than five milliseconds after fault inception.

CHAPTER 6

TEED CIRCUIT PERFORMANCE

6.1 Network Configurations

The performance of the fault generated noise protection scheme for a variety of practically encountered fault conditions is described in this next chapter. The two teed circuits studied and the relevant fault positions are shown in Fig. 6.1. The first is a symmetrical tee network with all three tee legs 80 km long (Fig. 6.1a). All three sources have a capacity of 20 GVA and there is no phase shift between the voltages at each end. This is an idealised configuration as it would be very unlikely to encounter a circuit such as this in practice. However, it is a good, simple case to clearly demonstrate the behaviour of this technique.

The second circuit has unequal tee leg lengths and different source capacities at each end (Fig. 6.1b). Also the source voltages at end P lag the end Q source voltages by 10°, and the end R voltages lag the end Q voltages by 5°. This is to represent some initial power flow around the network. The transmission line directly connecting end P to end R forms a feed around path. In practice, this connection is more likely to be made through a number of adjacent circuits rather than a single

transmission line. More emphasis is placed on the results for single phase to earth faults in this thesis as these are by far the most common encountered in practice.

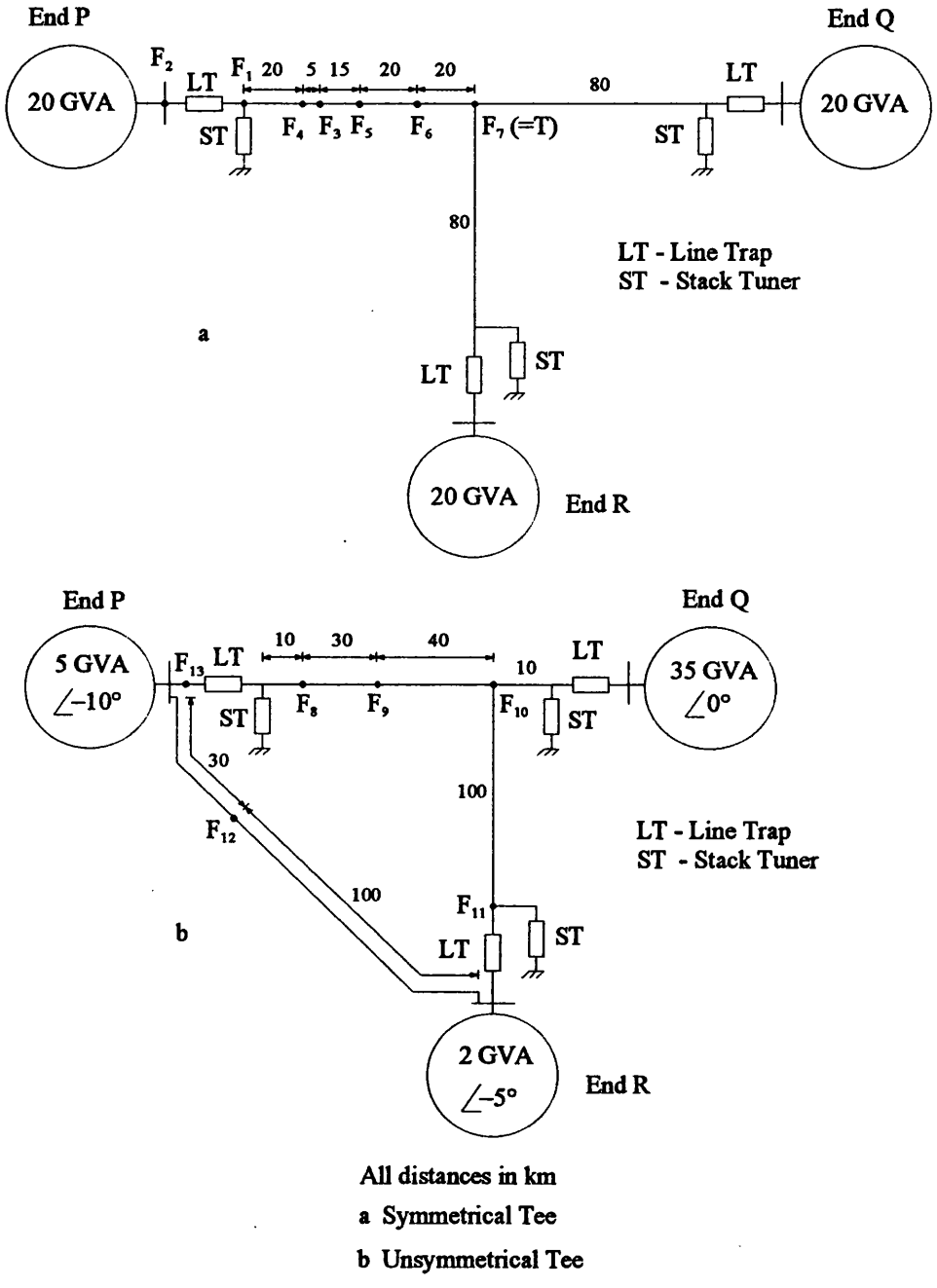


Fig. 6.1 - Teed circuit configurations

6.2 Typical Internal Fault Response

Following a fault, the high frequency signals that are set up travel along the transmission lines. The signals are in short bursts and are made up from the initial burst and its reflections from any impedance discontinuities, ie the line ends, the fault point and the tee point. This can clearly be seen by closely examining the responses for a typical fault. An internal phase a to earth fault is applied 2.5 ms after the start of the simulations very near to a voltage zero, 25 km from end P, F_3, on the symmetrical tee circuit of Fig. 6.1a.

The three phase voltage waveforms at end P show the reduction in the faulted phase voltage and that few transients are set up as the fault is applied very near to a voltage zero (Fig. 6.2a). Additional transients can be seen at approximately 19.6 ms, 24.9 ms, 38.9 ms and 45.6 ms. These appear twice per 50 Hz cycle and are due to the arc restriking as the fault current passes through zero. The typical dc offset of the current waveform associated with voltage zero faults is also shown in Fig. 6.2b. The faulted phase current is significantly greater than the unfaulted phase currents as expected.

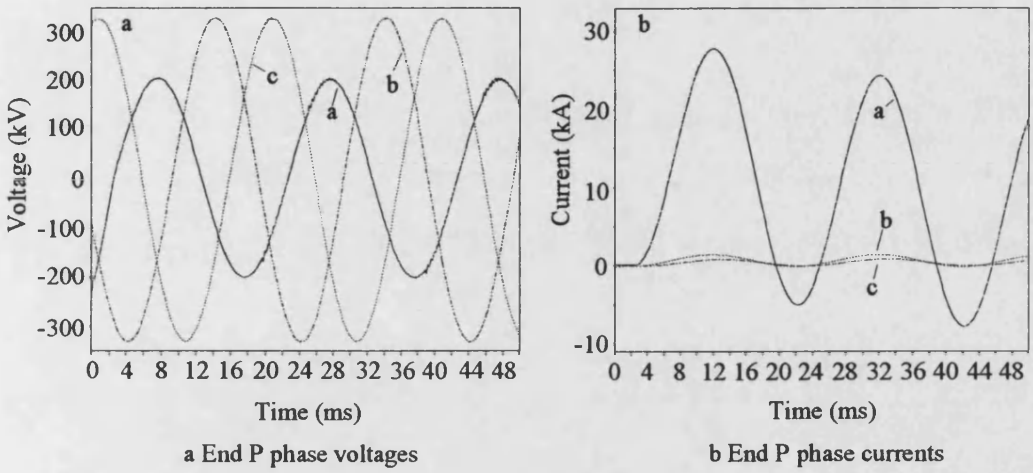
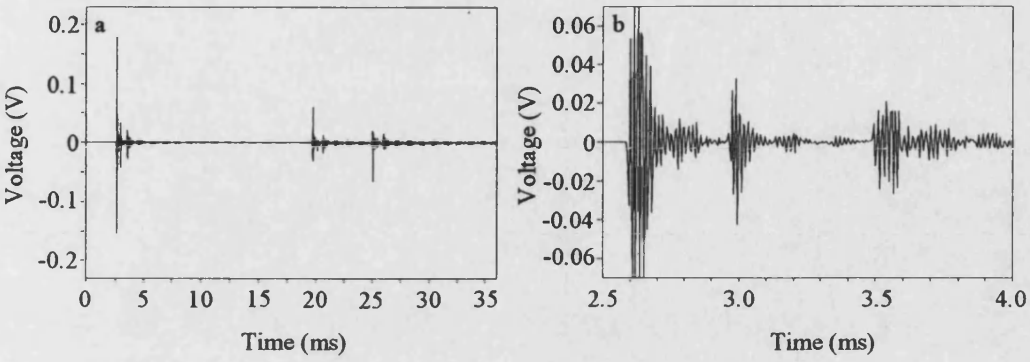


Fig. 6.2 - Typical internal fault phase voltages and currents

The stack tuners are specifically designed to capture the HF disturbances generated by the arcing fault. The mode V_x stack tuner output at end P contains a number of different bursts (Fig. 6.3a). The initial burst is at fault inception and the two other significant bursts are caused by the arc restrikes. Closer examination of the first burst reveals that it is made up from several components (Fig. 6.3b). These are the reflections of the fault generated signals from the impedance discontinuities of the circuit. Table 6.1 identifies the route taken by the first few signals. There are also reflections back from the fault point at approximately 2.75 ms and 2.92 ms, but they are swamped by the stronger reflections.



a End P mode V_x stack tuner output b Magnified End P mode V_x stack tuner output

Fault inception, $t_f = 2.5$ ms

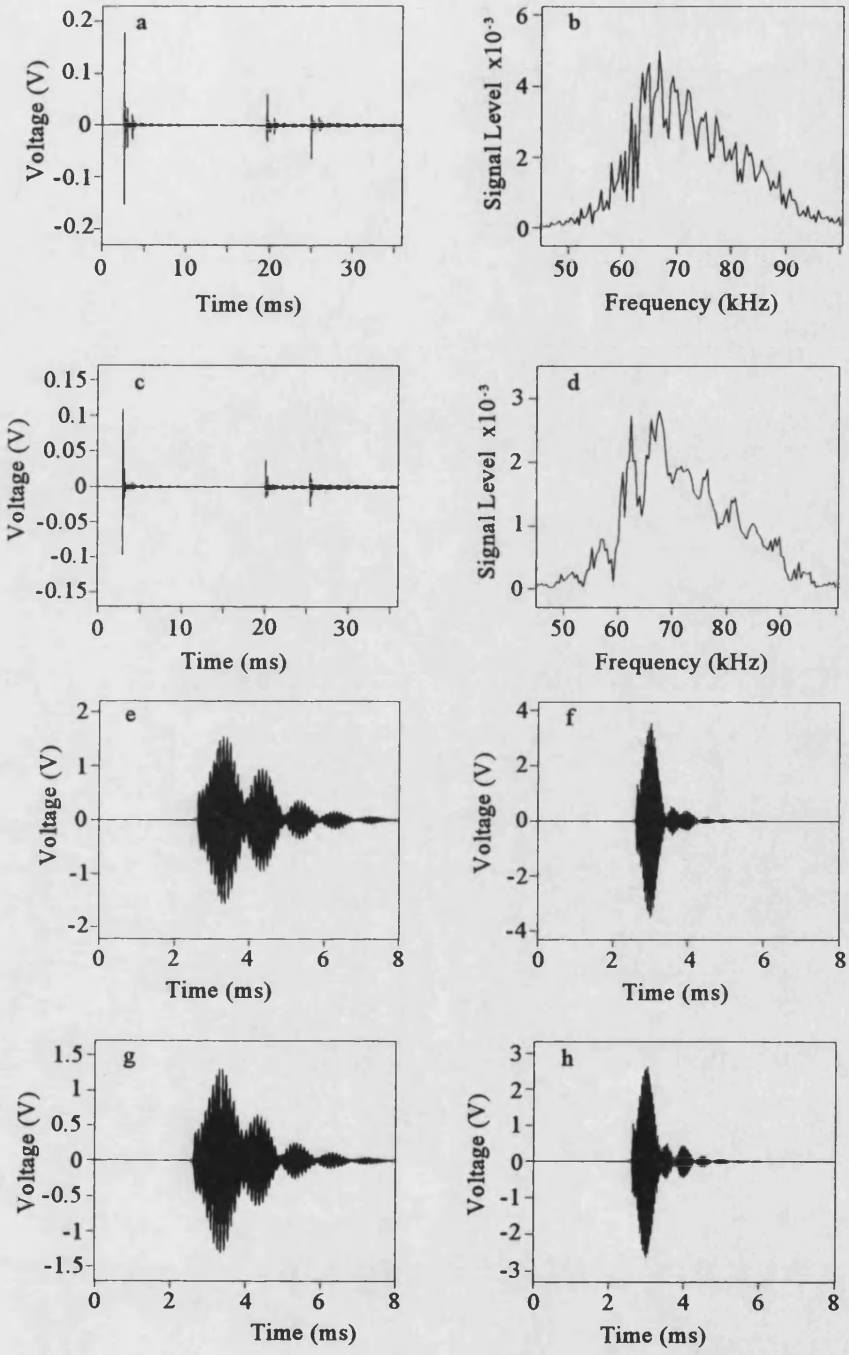
Fig. 6.3 - End P stack tuner output

Table 6.1 - Components of initial burst

Time (ms)	Travel time (ms)	Distance travelled (km)	Route taken
2.590	0.090	25	$F_3 \rightarrow P$
2.960	0.460	135	$F_3 \rightarrow T \rightarrow P$
3.135	0.635	185	$F_3 \rightarrow T \rightarrow P \rightarrow F_3 \rightarrow P$
3.335	0.835	245	$F_3 \rightarrow T \rightarrow F_3 \rightarrow T \rightarrow P$
3.495	0.995	295	$F_3 \rightarrow Q/R \rightarrow P$
3.670	1.170	345	$F_3 \rightarrow Q/R \rightarrow P \rightarrow F_3 \rightarrow P$
3.870	1.370	405	$F_3 \rightarrow Q/R \rightarrow F_3 \rightarrow T \rightarrow P$

A full breakdown of the signals that both modes use to formulate the trip decision is given in Figs. 6.4 and 6.5. The stack tuner outputs show the initial disturbance and the subsequent arc restrikes (Fig. 6.4a,c). As the fault is internal to the protected zone, the HF signals have not passed through the line traps and so there is no attenuation of either mode around the centre frequency of 75 kHz (Fig. 6.4b,d). The narrow bandpass filters of both modes, therefore, detect signals of a fairly similar strength (Fig. 6.4e-h). After being enhanced to make them proportional to the spectral power of the input signal, the operate outputs of both modes are found to be approximately twice the magnitude of the corresponding restraint outputs (Fig. 6.5a-d). This is a direct result of the operate filters having twice the bandwidth of the restraint filters.

Close examination of Fig. 6.5b,d reveals that the rising ratio algorithm forces the outputs to zero at 4.5 ms to eliminate any errors as the moving average calculations decay towards zero. The discrimination ratios of the two modes therefore settle at just above two causing the trip counters to exceed the trip level 2.98 ms and 3.00 ms after fault inception (Fig. 6.5e-h). Therefore, an output to trip the line circuit breakers would be issued after 2.98 ms (not including the processing time).



a Mode V_x stack tuner output

b Frequency spectrum of a

c Mode V_y stack tuner output

d Frequency spectrum of c

e Mode V_x restraint filter output

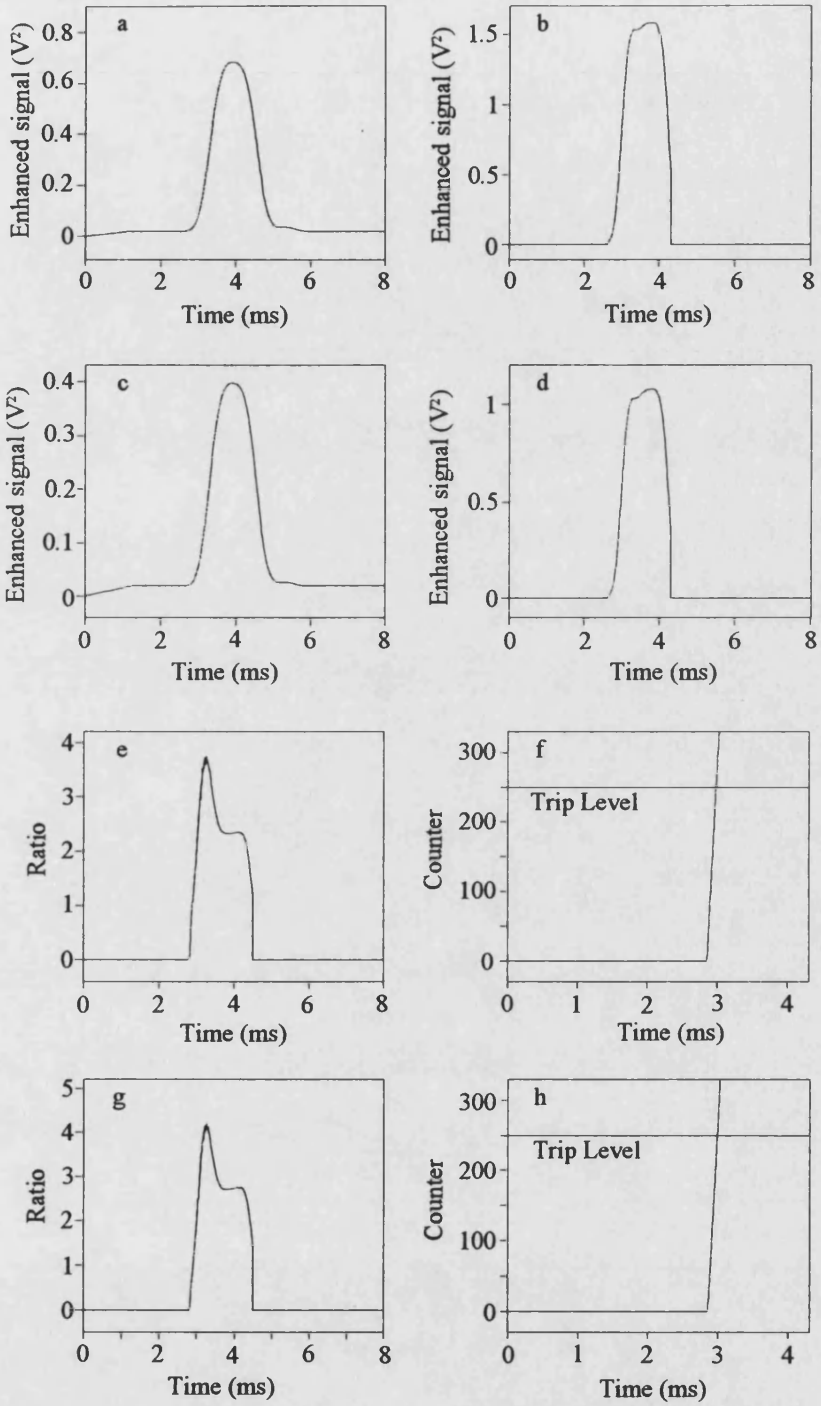
f Mode V_x operate filter output

g Mode V_y restraint filter output

h Mode V_y operate filter output

Fault inception, t_f = 2.5 ms

Fig. 6.4 - Typical internal fault response



a Mode V_x enhanced restraint filter output

b Mode V_x enhanced operate filter output

c Mode V_y enhanced restraint filter output

d Mode V_y enhanced operate filter output

e Mode V_x discrimination ratio

f Mode V_x trip counter output

g Mode V_y discrimination ratio

h Mode V_y trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.5 - Typical internal fault response

6.3 Typical External Fault Response

The same fault is applied on the busbar at end P, just behind the line trap, to give an external fault response (F_2 in Fig. 6.1a). The faulted phase voltage collapses when the fault is applied (after 2.5 ms) and as the fault point is very close, the subsequent trace is essentially the arc voltage (Fig. 6.6a). The non linear arc behaviour is evident, with the distortion at the fault current zero crossing points being clearly visible. Again, the faulted phase current is almost fully offset as the inception angle is very close to zero (Fig. 6.6b).

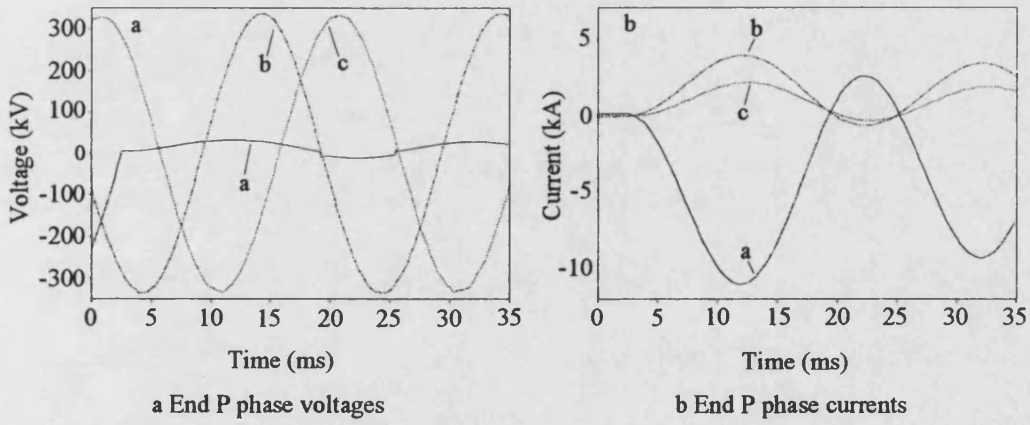


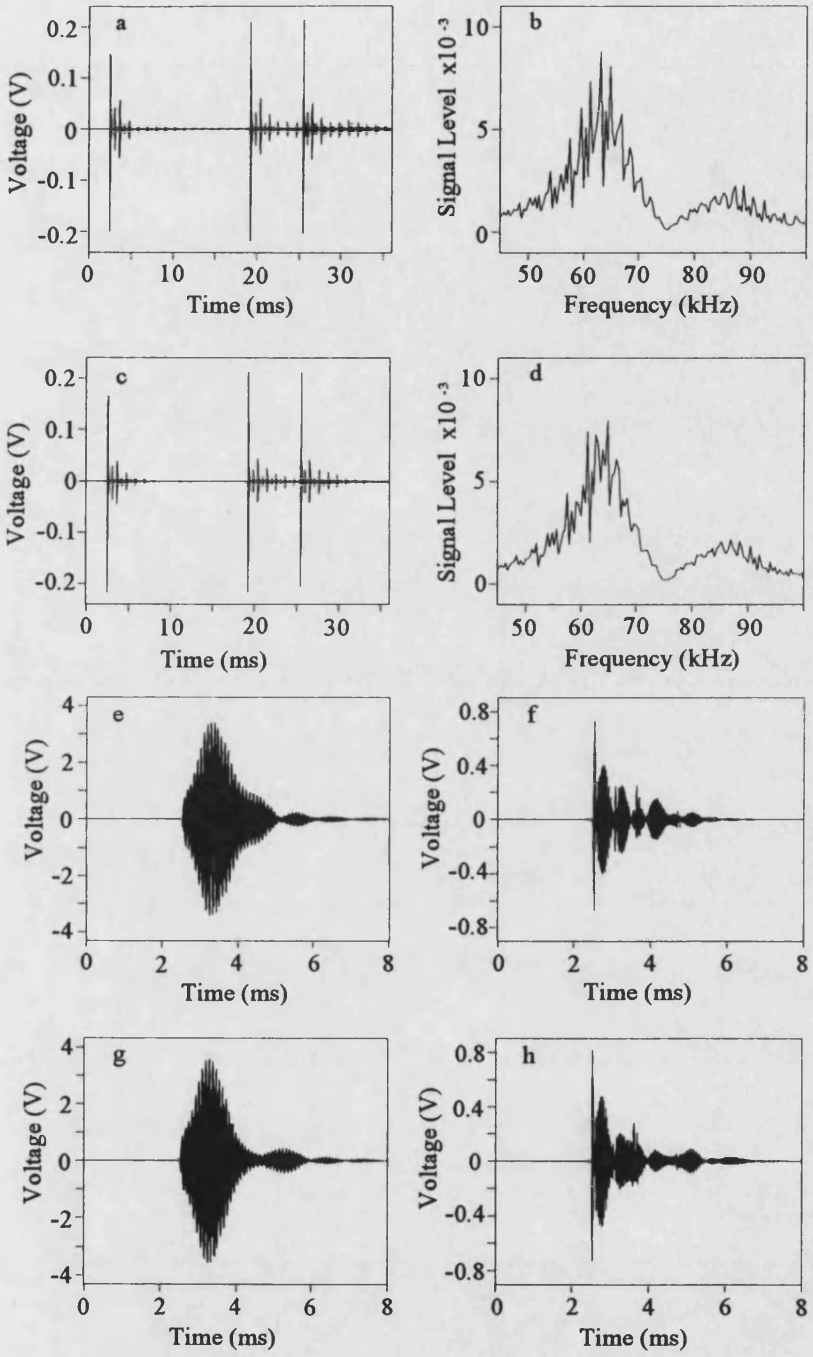
Fig. 6.6 - Typical external fault phase voltages and currents

The two modal stack tuner signals appear to be much simpler than the internal fault case (Fig. 6.7a,c), but this is mainly because the fault is at one end and so the reflections are only from the tee point and the far end terminals. In addition, the tee point is 80 km from the fault and the other two ends are both 160 km away and so some of the reflections are superimposed, further reducing the number of signals

present. The additional HF signals generated by the arc restrikes are also evident. The severe attenuation of the HF signals by the line trap can clearly be seen in the frequency spectra of the stack tuner outputs, demonstrating that this is an external fault (Fig. 6.7b,d).

The signals detected by the operate filters are, therefore, much less than those measured at the lower restraint frequency (Fig. 6.7e-h). The spectral energy content of the restraint signals is considerably greater than that of the operate signals and this is shown in the corresponding enhanced filter outputs (Fig. 6.8a-d). This should give rise a very low discrimination ratio. For the V_x mode, the ratio peaks at 0.122 very shortly after fault inception, but it starts to rise again as 5 ms is approached (Fig. 6.8e). Examination of the enhanced outputs shows that both of these are decaying at this time. The rise in the ratio is caused by these two signals falling at different rates (see section 5.6.1). The rising ratio algorithm cuts in at 5.38 ms and stops the ratio rising any further and so the trip counter remains at zero (Fig. 6.8f). A similar situation occurs with the V_y mode and again the counter remains at zero (Fig. 6.8g,h).

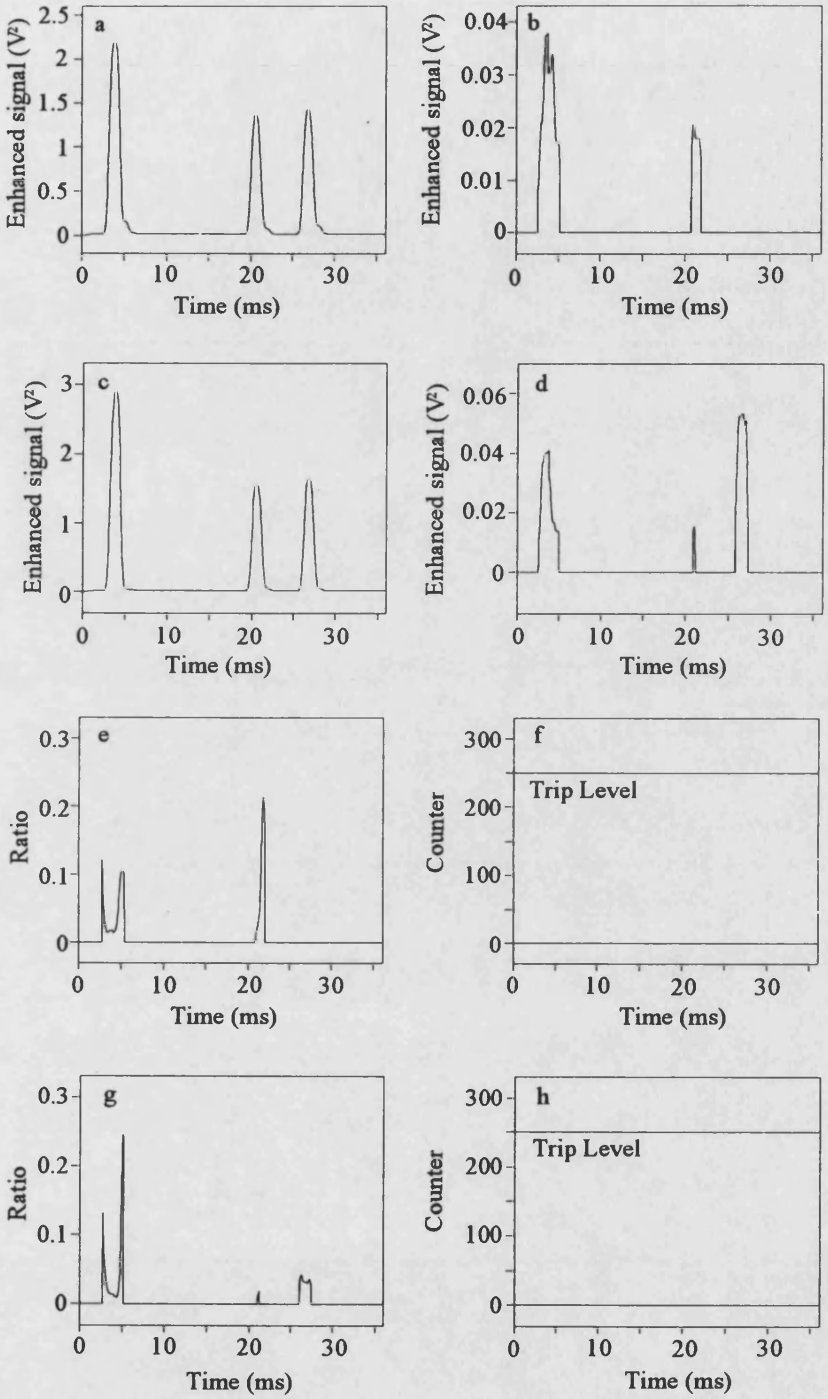
The decaying enhanced outputs of mode V_x also cause the discrimination ratio to peak at just over 0.2 after the first arc restrike. Again the rising ratio algorithm forces the output to zero. The decision logic counting algorithm is included to ensure that the relay performs correctly even when there are these slight errors in the discrimination ratio calculation.



a Mode V_x stack tuner output
b Frequency spectrum of a
c Mode V_y stack tuner output
d Frequency spectrum of c
e Mode V_x restraint filter output
f Mode V_x operate filter output
g Mode V_y restraint filter output
h Mode V_y operate filter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.7 - Typical external fault response



a Mode V_x enhanced restraint filter output

b Mode V_x enhanced operate filter output

c Mode V_y enhanced restraint filter output

d Mode V_y enhanced operate filter output

e Mode V_x discrimination ratio

f Mode V_x trip counter output

g Mode V_y discrimination ratio

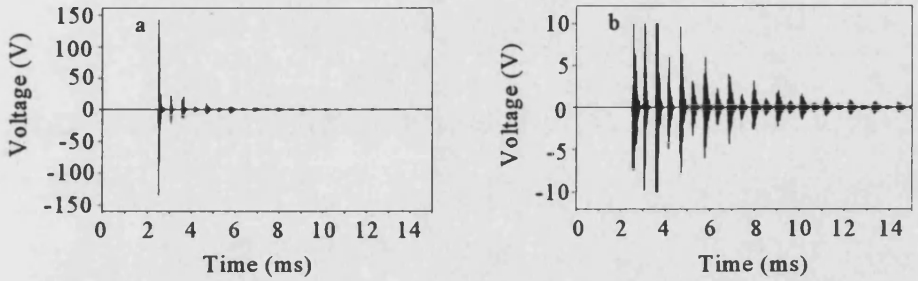
h Mode V_y trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.8 - Typical external fault response

6.4 Signal Clipping

The large dynamic range of the signals measured at the output of the stack tuners requires them to be clipped to ± 10 V (see section 5.2). This signal limiting means that for certain faults, the input signal is slightly corrupted by the reduction in its spectral power. This can be demonstrated by looking at a phase a to earth voltage maximum fault, just in front and just behind the line trap at one end.



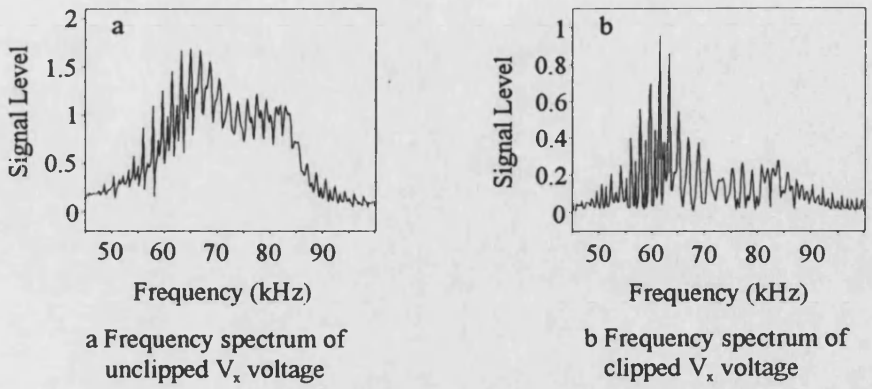
a Unclipped V_X voltage

b Clipped V_x voltage

Fault inception, $t_f = 2.5$ ms

Fig. 6.9 - Internal fault stack tuner output

Figure 6.9 shows the unclipped and clipped first aerial mode signal, V_x, for an internal fault just in front of the line trap (F_1 in Fig. 6.1a). The very large initial burst of the unclipped signal is clearly visible along with the effect of limiting these signals. The decay of the bursts of the signals can also be seen. The frequency spectra gives a clearer indication of the clipping distortion (Fig. 6.10). The overall signal level is clearly reduced and appears as though it may affect the performance of the protection scheme.

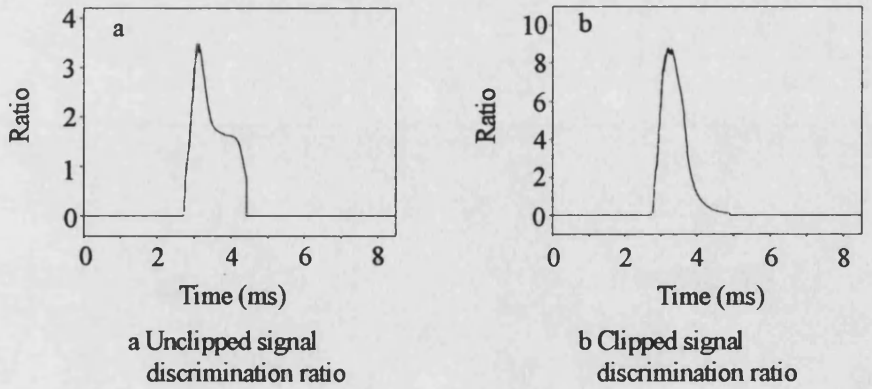


a Frequency spectrum of unclipped V_x voltage

b Frequency spectrum of clipped V_x voltage

Fig. 6.10 - Internal fault frequency spectra

The position of the restraint filter has been carefully chosen to counteract the distortion due to the clipping action. This can be demonstrated by examining the discrimination ratio outputs of these two cases (Fig. 6.11). The ratio peaks at approximately 3.5 for the unclipped case, but it reaches 9 when the signal is limited. This is due to the restraint filters' output also being reduced by the clipping and the larger bandwidth of the operate filter.

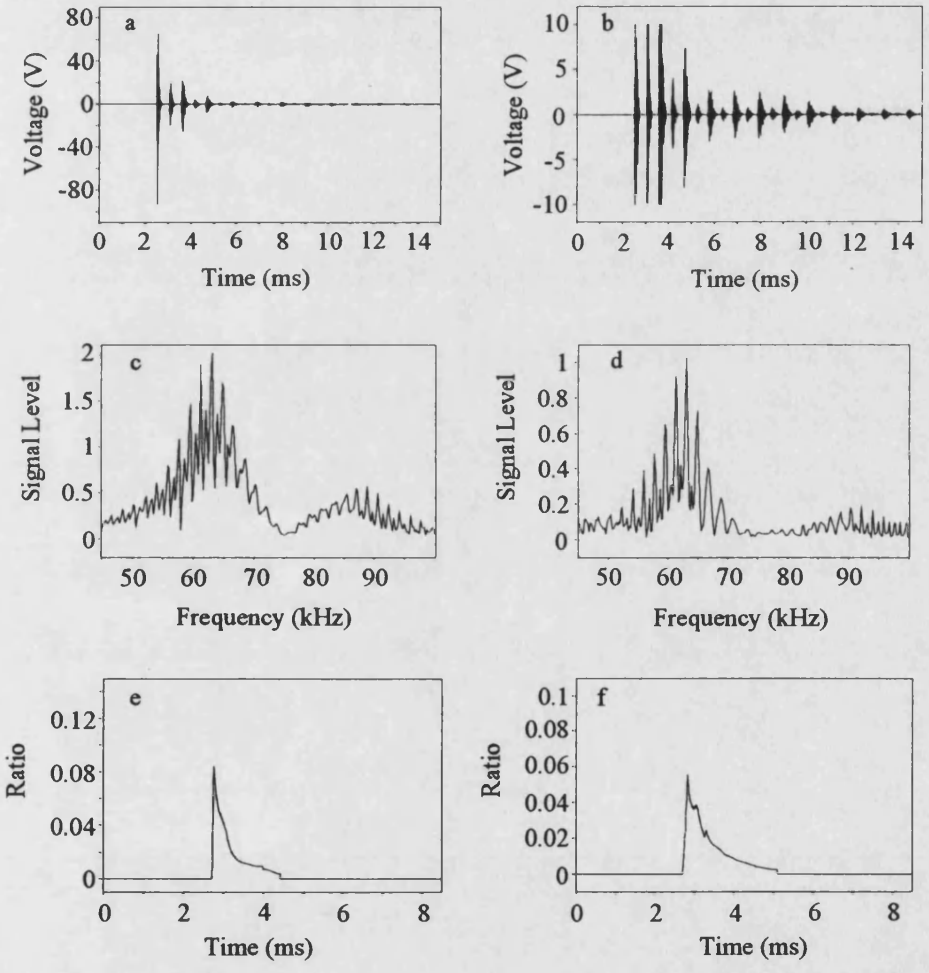


a Unclipped signal discrimination ratio

b Clipped signal discrimination ratio

Fig. 6.11 - Internal fault discrimination ratios

For the external fault case, F_2 in Fig. 6.1a, the aerial mode signal V_x, again has to be clipped (Fig. 6.12a,b), causing a reduction in the spectral power and some distortion (Fig. 6.12c,d). The operate filter output is very small in both cases, but because of the positioning of the filters, there is only a slight difference in the discrimination ratios that are calculated (Fig. 6.12e,f).



a Unclipped V_x voltage

b Clipped V_x voltage

c Frequency spectrum of unclipped V_x voltage

d Frequency spectrum of clipped V_x voltage

e Unclipped signal discrimination ratio

f Clipped signal discrimination ratio

Fault inception, $t_f = 2.5$ ms

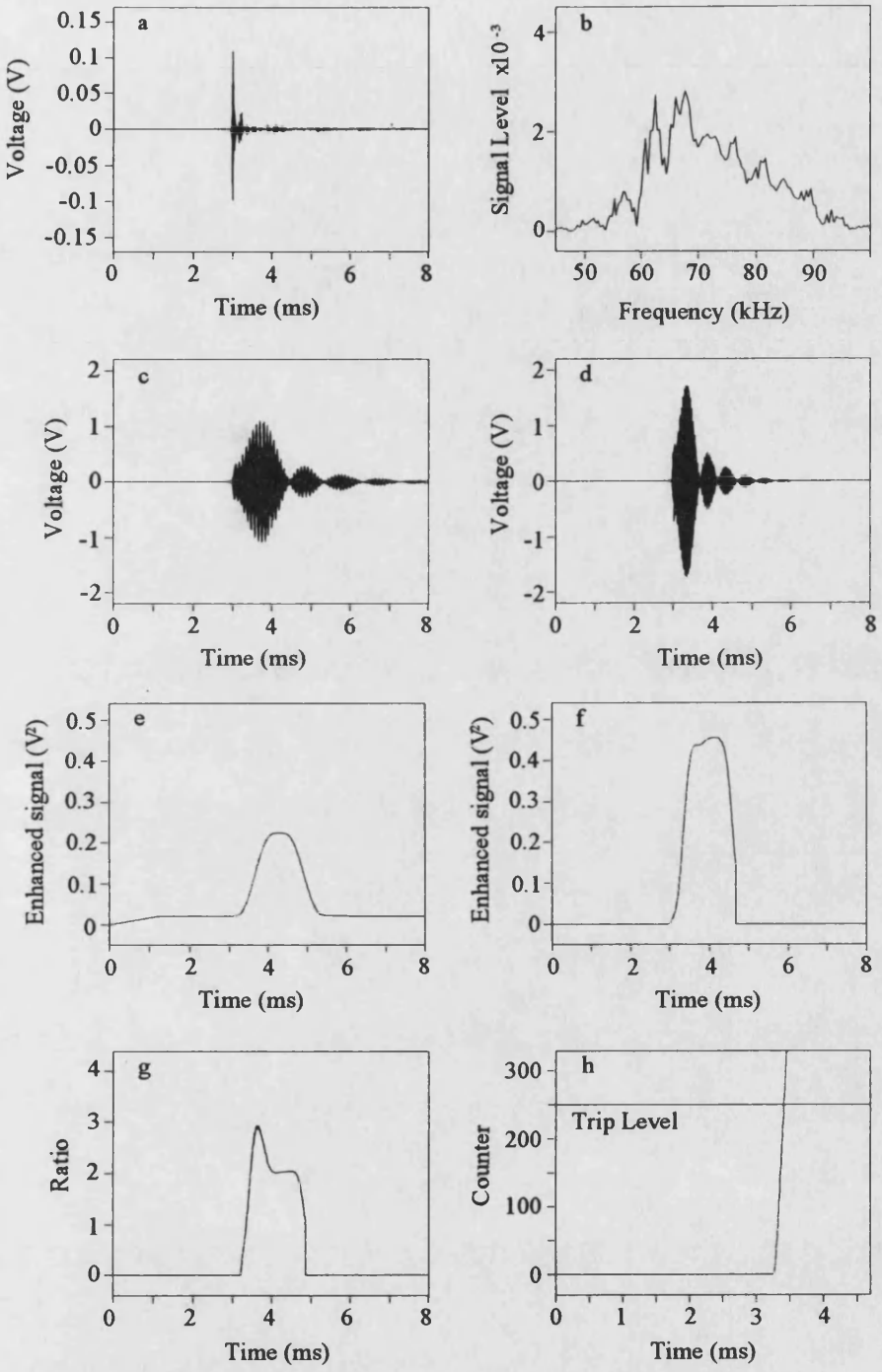
Fig. 6.12 - External fault

6.5 The Effect of Fault Inception Angle

The fault inception angle has a significant effect on the post-fault signals that are generated. It principally influences the amount of travelling wave type voltage components that are set up and the degree of dc offset on the current waveform. This section examines a number of different faults to demonstrate its effect.

6.5.1 Internal Faults

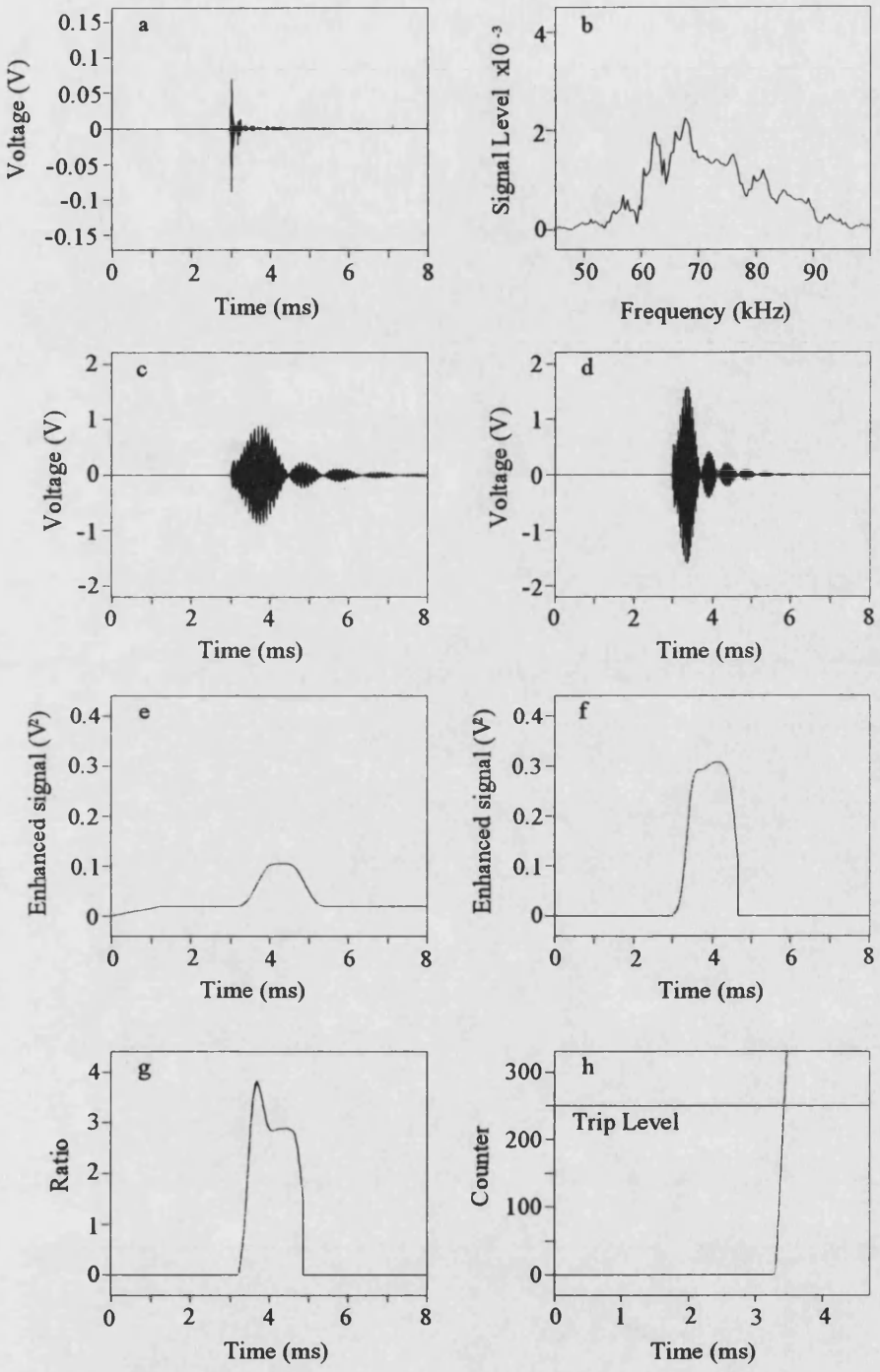
An internal phase a to earth near voltage zero fault at F_3 in Fig. 6.1a, has already been examined in some depth in section 6.2. This showed that only a small amount of HF voltage signals were generated and there was a large dc offset on the faulted phase current (Fig. 6.2). The signals captured by the stack tuners and the intermediate outputs were shown for both modes at end P in Figs. 6.4 and 6.5. The two modal outputs for end Q are shown in Figs. 6.13 and 6.14 and comparing them with the outputs at end P shows that there are some slight differences.



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.13 - Internal near 0° fault mode V_x response at end Q



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.14 - Internal near 0° fault mode V_y response at end Q

The reduction in the signal magnitudes at end Q has been caused by the attenuation of the line and the tee point impedance discontinuity. The signals arrive at end Q later as they have a further distance to travel. The different reflections can also be seen and are further emphasised by the filter outputs (Figs. 6.13c,d, 6.14c,d). Although the strengths of the signals have been reduced, the relative magnitudes of the enhanced filter outputs remain approximately constant (Figs. 6.13e,f, 6.14e,f) and so there is very little change to the discrimination ratio outputs (Figs. 6.13g, 6.14g). The end R signals are not shown as they are identical to the end Q waveforms. This is because of the symmetry of the circuit being studied.

Increasing the fault inception angle to 45° whilst keeping all of the other parameters constant, has a significant effect on the signals generated. Figure 6.15 shows the larger voltage disturbances, and the lower dc offset on the current waveform.

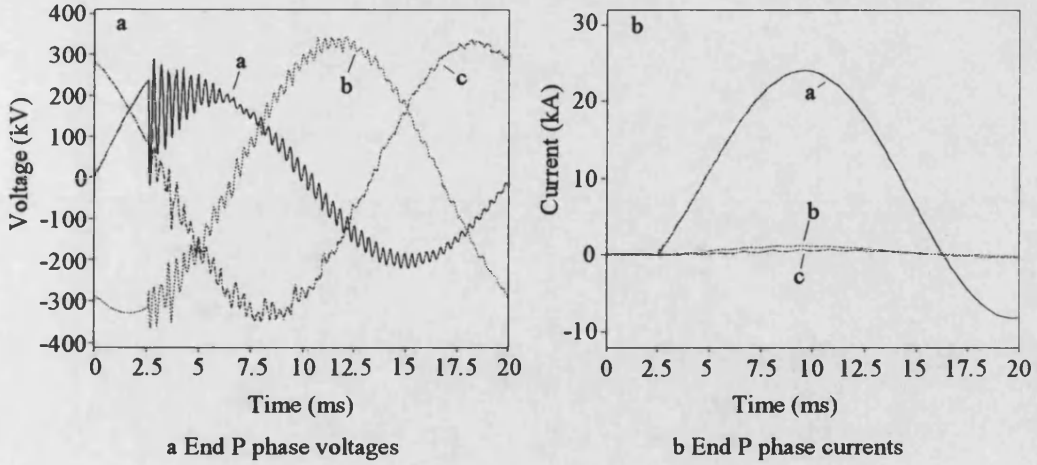
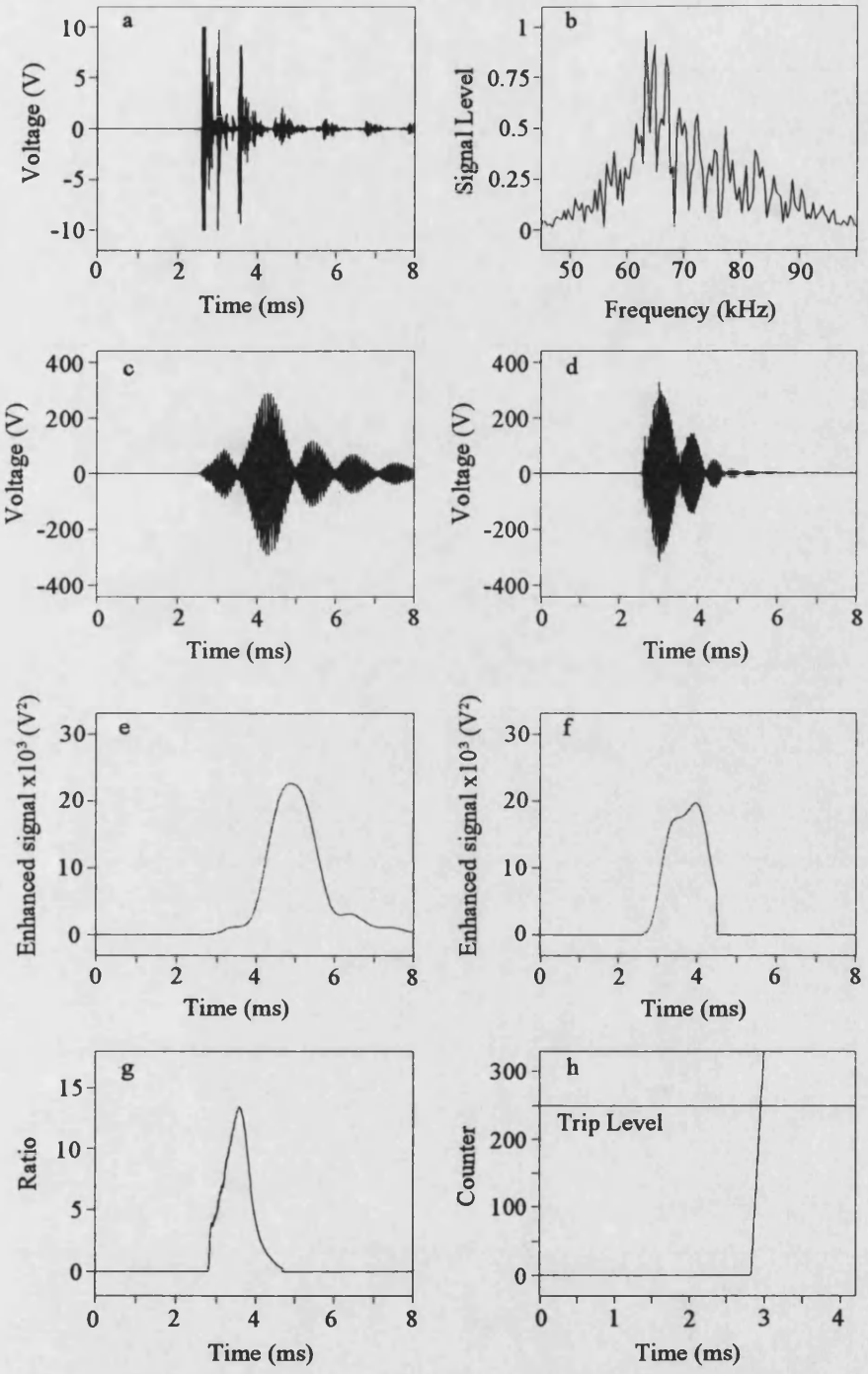


Fig. 6.15 - Internal 45° fault phase voltages and currents

Consequently, there is a considerable increase in the amount of HF components present and the mode V_x signals at end P are shown in Fig. 6.16. The stack tuner output has been clipped to ± 10 V by the signal limiter and so there is some distortion which can be seen in the frequency domain (Figs. 6.16a,b). The filter outputs are approximately two orders of magnitude larger than the near voltage zero fault case (Figs. 6.16c,d) and the enhanced filter outputs are up to four orders of magnitude larger (Figs. 6.16e,f). The discrimination ratio is very much greater than unity, but this has also been increased by the effect of the clipping action (Fig. 6.16g).

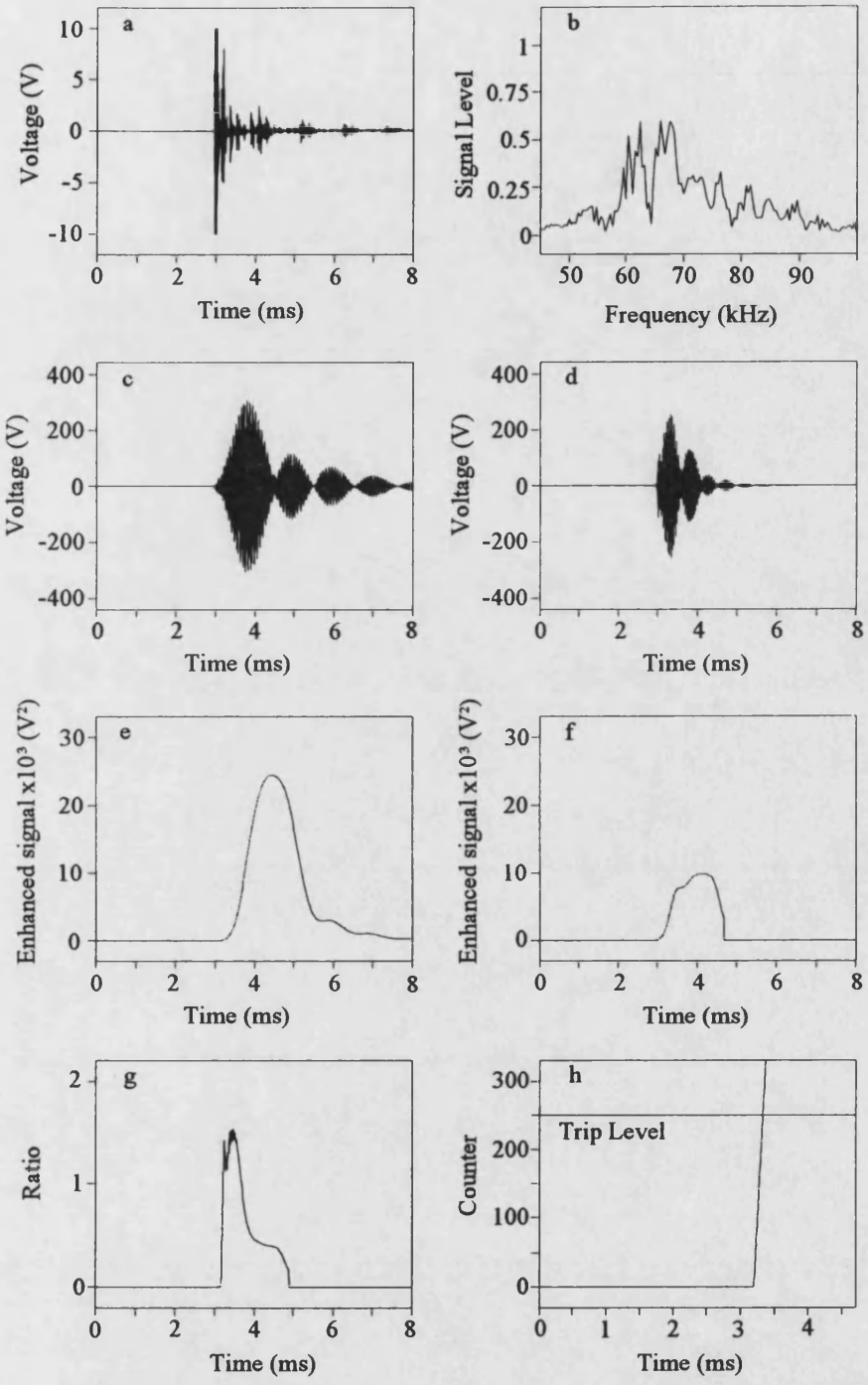
At end Q, the signals have similar magnitudes to those at end P, although they are delayed by the additional travel time (Fig. 6.17). The line attenuation also means that less clipping is required, reducing the amount of distortion (Figs. 6.17a,b). The filter outputs are therefore, marginally lower and the discrimination ratio peaks at approximately 1.5 (Figs. 6.17c-g). A trip decision is then given 0.83 ms after fault inception.



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.16 - Internal 45° fault mode V_x response at end P



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.17 - Internal 45° fault mode V_x response at end Q

Raising the inception angle to 90° (ie voltage maximum), increases the amount of voltage transients further. There is practically no dc offset on the current waveform and this is shown in Fig. 6.18.

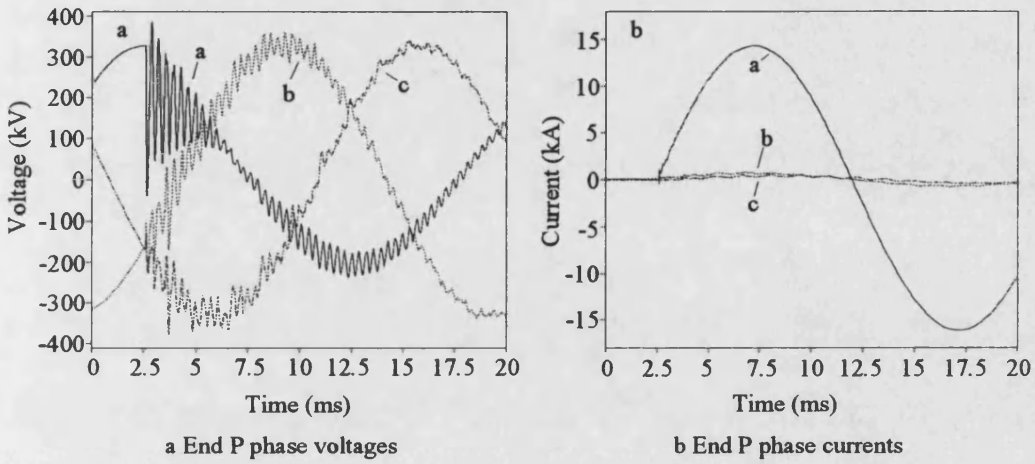
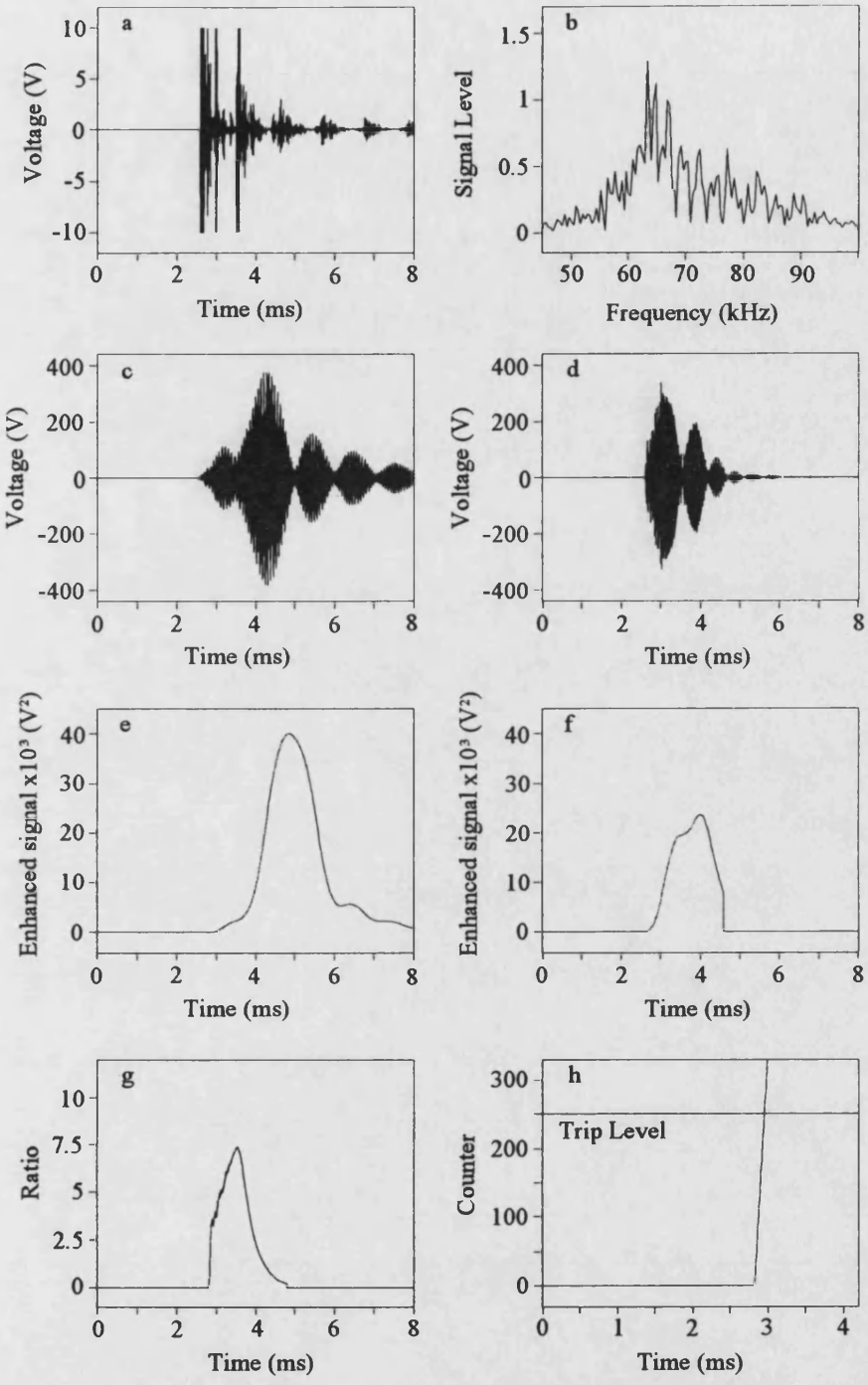


Fig. 6.18 - Internal 90° fault phase voltages and currents

The stack tuner therefore captures greater quantities of HF noise but they are again limited to ± 10 V (Fig. 6.19a). The increase in the signal magnitudes associated with the larger fault inception angle are therefore minimised. The basic nature of the signals remains the same with the enhanced filter outputs this time reaching approximately 40000 V^2 (Figs. 6.19c,d). A discrimination ratio of approximately 7.5 is achieved and a trip decision is made 0.45 ms after fault inception.

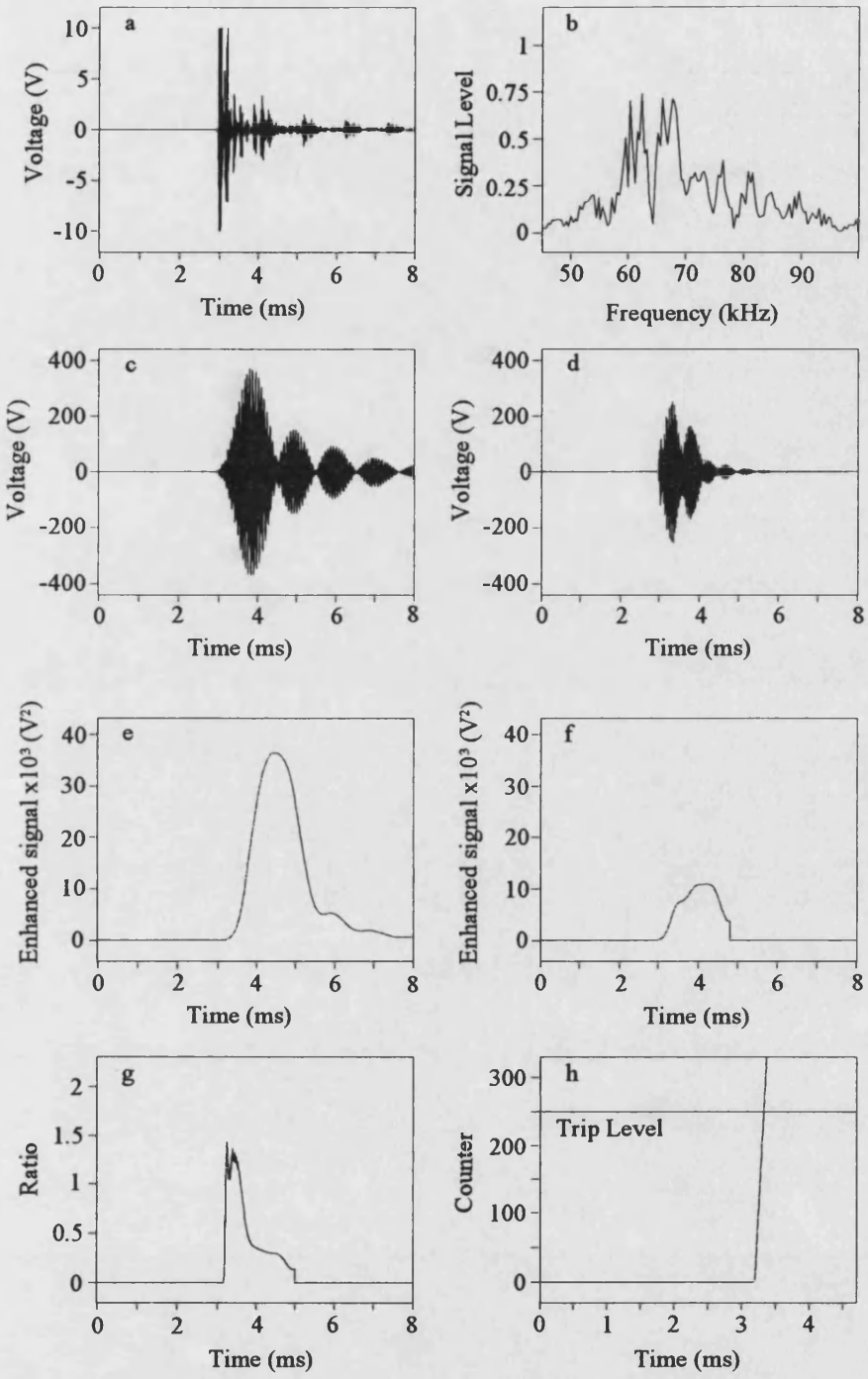
The waveforms are again similar at end Q for the same case (Fig. 6.20). As expected the additional attenuation and delays are also present.



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.19 - Internal 90° fault mode V_x response at end P



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.20 - Internal 90° fault mode V_x response at end Q

The time to trip after fault initiation is not significantly affected by the fault inception angle and this is shown in Table 6.2. This is inspite of the four orders of magnitude differences in the signal levels for near voltage zero and voltage maximum faults. The near voltage zero fault case takes fractionally longer to trip because the moving average algorithm has more of an effect as the enhanced filter output values are relatively small.

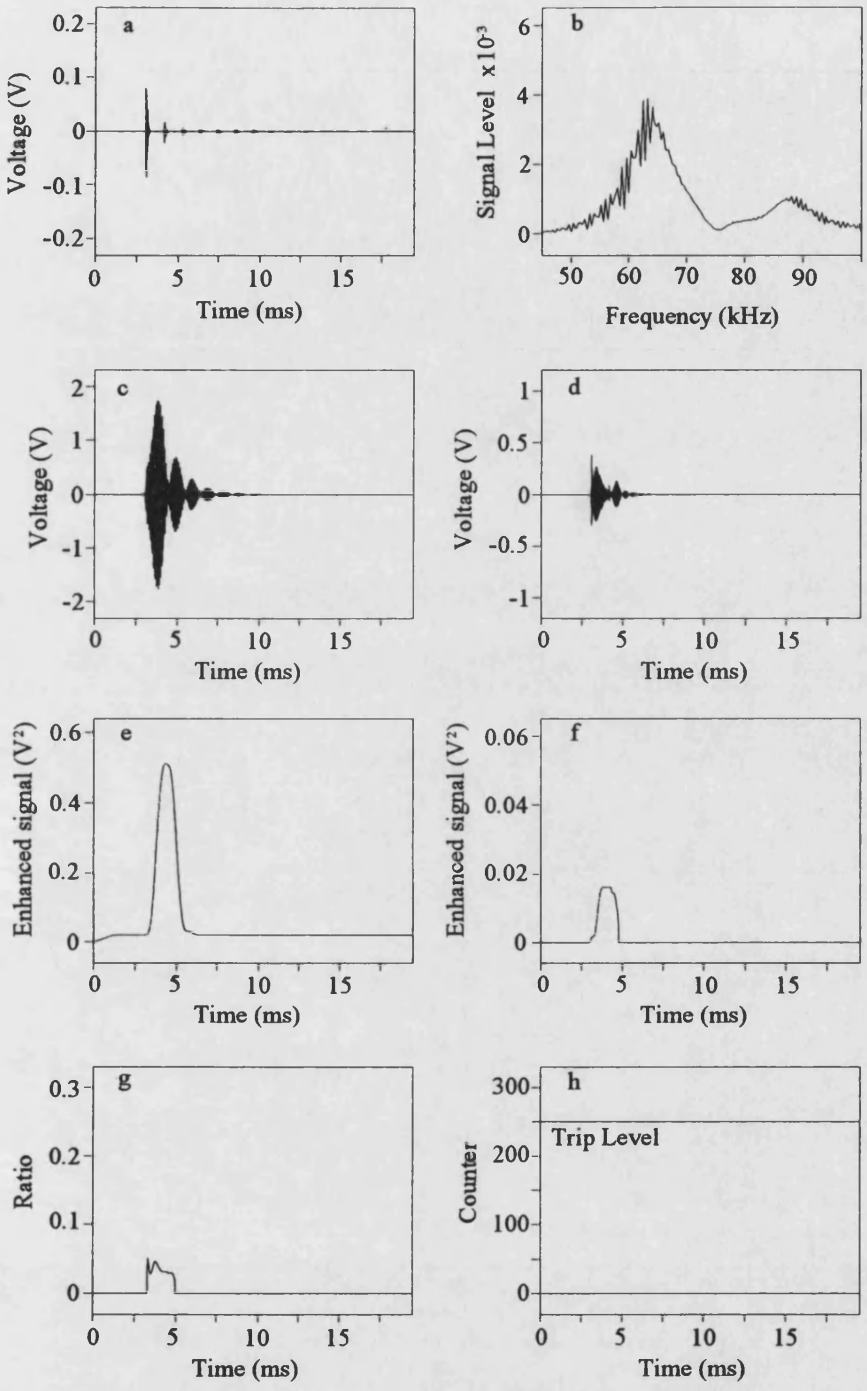
Table 6.2 - The effect of fault inception angle

Fault characteristics Note: Fault angle is the angle of V_a at end P			Time to trip after fault inception (ms)			
			End P		End Q	
Position	Angle	Type	Mode V_x	Mode V_y	Mode V_x	Mode V_y
F_3	0°	A-E	0.480	0.495	0.910	0.930
F_3	45°	A-E	0.455	0.450	0.830	0.830
F_3	90°	A-E	0.450	0.450	0.825	0.830

6.5.2 External Faults

A phase a to earth fault is applied near to a voltage zero at F_2 in Fig. 6.1a. This is just behind the line trap at end P and so is external to the protected zone. The mode V_x and V_y waveforms at end P have already been examined in section 6.3 (Figs. 6.7, 6.8). The enhanced restraint filter outputs peak at below 3 V^2 , the enhanced operate filter outputs reach approximately 0.04 V^2 and so this gives rise to very low discrimination ratios for the two modes as expected. Figures 6.21 and 6.22 show the outputs for both modes at end Q.

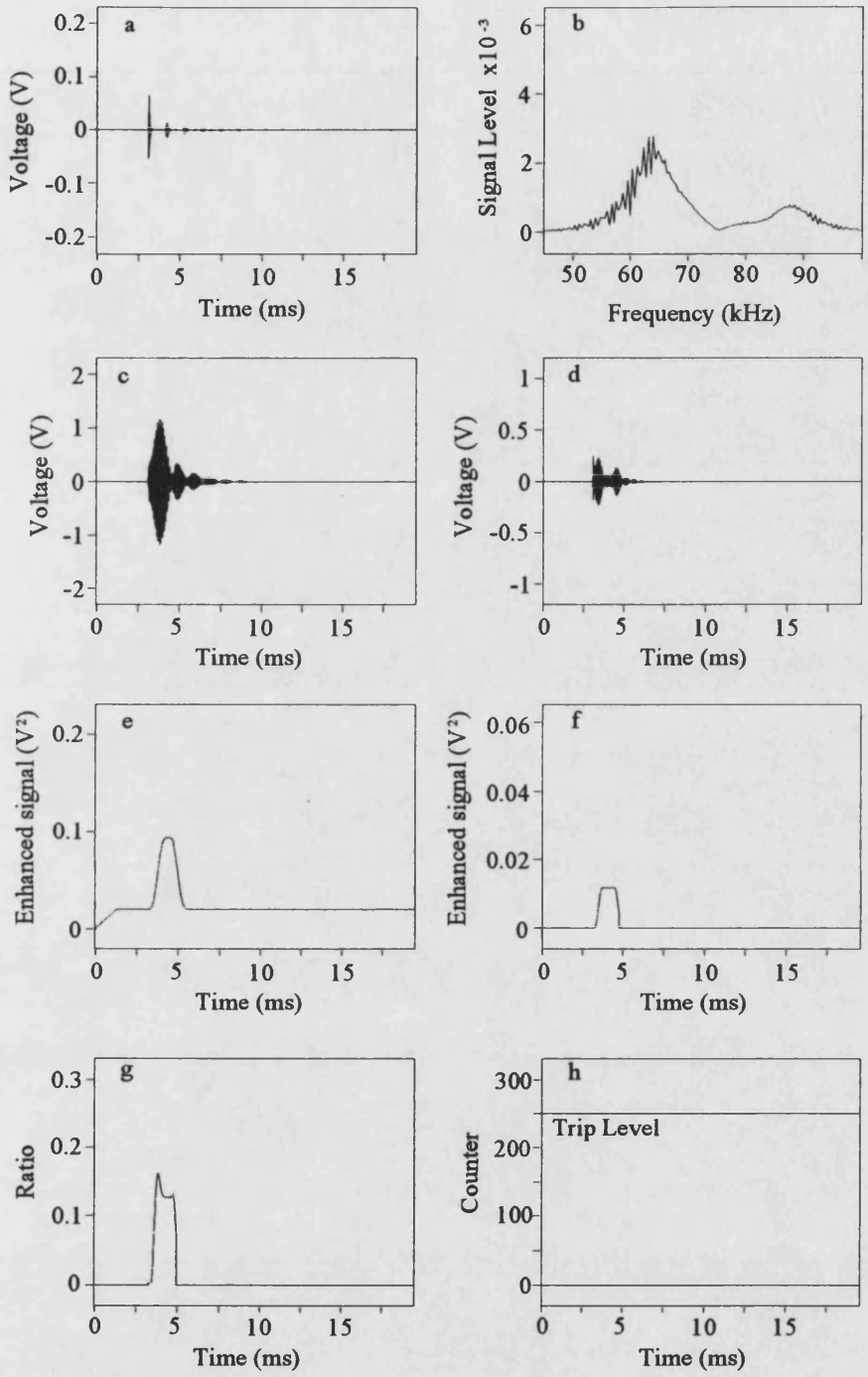
The waveforms are essentially the same as the end P waveforms. The magnitudes are reduced by the waves propagation through the network along with the associated increase in the travel time. The stack tuner outputs contain slightly different reflections due to the change in position relative to the fault position (Figs. 6.21a, 6.22a) and this is also evident in the filter outputs (Figs. 6.21c,d, 6.22c,d). In all of the cases, there is severe attenuation of the narrow frequency band around 75 kHz as expected. The discrimination ratios remain well below unity (Figs. 6.21g, 6.22g) and so no trip decisions are given (Figs. 6.21h, 6.22h).



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.21 - External near 0° fault mode V_x response at end Q



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

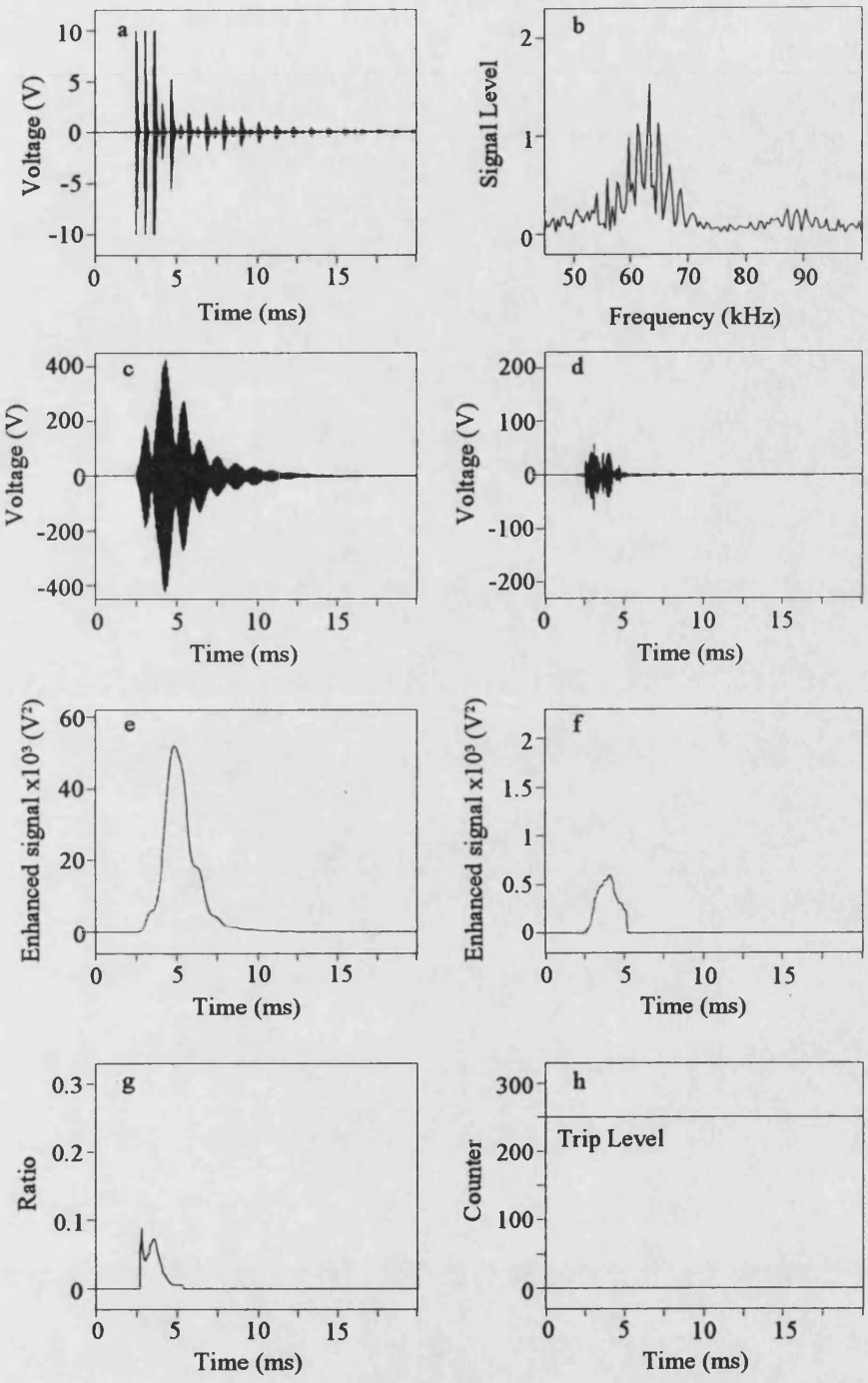
Fault inception, $t_f = 2.5$ ms

Fig. 6.22 - External near 0° fault mode V_y response at end Q

The mode V_x stack tuner output at end P is considerably larger for a fault inception angle of 45° (Fig. 6.23a). The signal has to be clipped to ± 10 V but this does not significantly distort its frequency domain profile (Fig. 6.23b). The enhanced restraint filter output exceeds 50000 V^2 while the operate output reaches approximately 600 V^2 (Figs. 6.23e,f). The discrimination ratio peaks at just below 0.1 and no trip decision is issued (Figs. 6.23g,h).

Figure 6.24 shows the mode V_x outputs at end Q for the same fault case. Again the slight differences are due to the extra distance travelled by the end Q signals and the trip counter remains at zero.

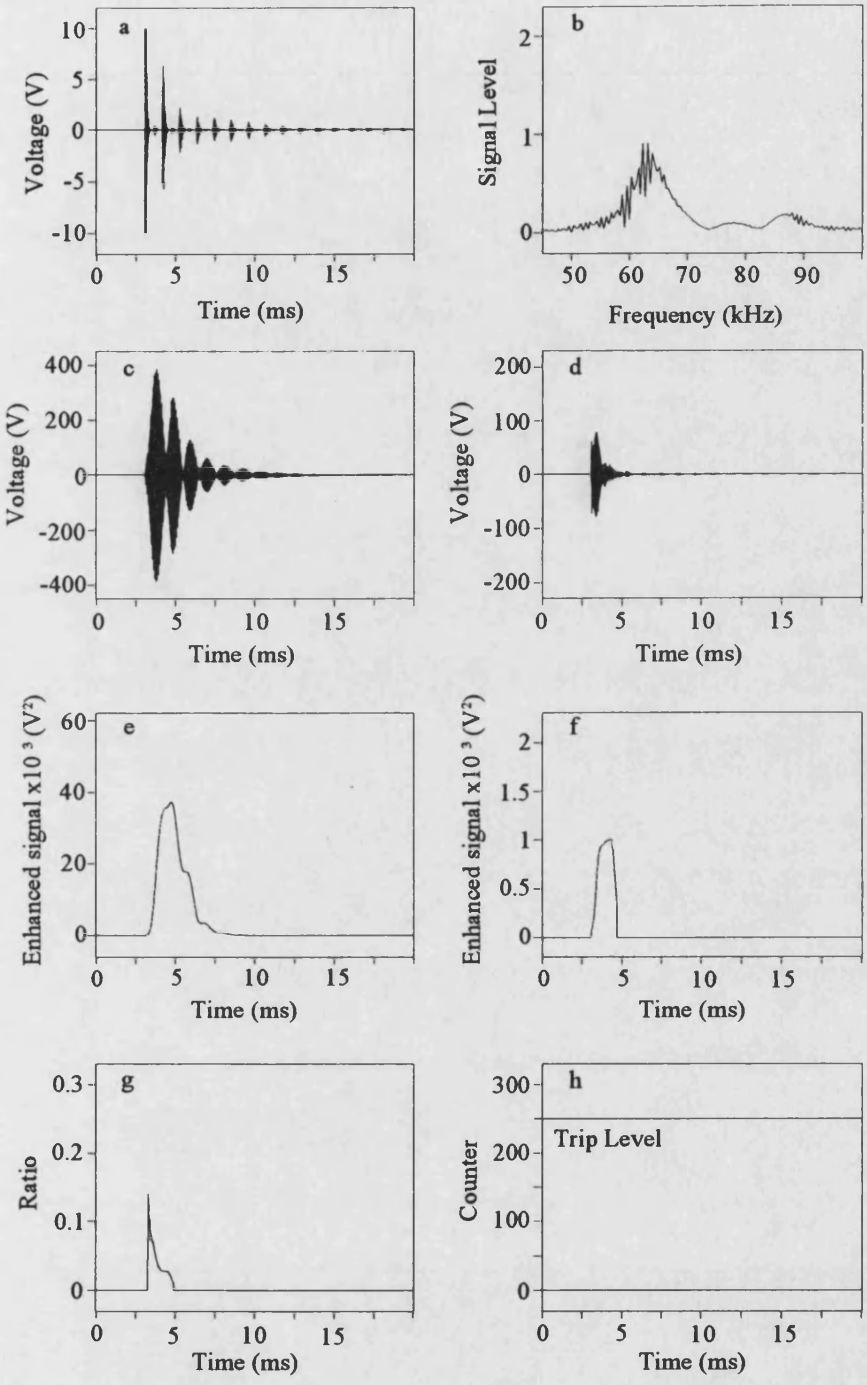
Increasing the fault inception angle to 90° (ie voltage maximum) does not have any major effects on the waveforms. Figures 6.25 and 6.26 show the mode V_x outputs at ends P and Q respectively. The signal levels are only increased by the additionally generated HF components and the trip counters both remain at zero.



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

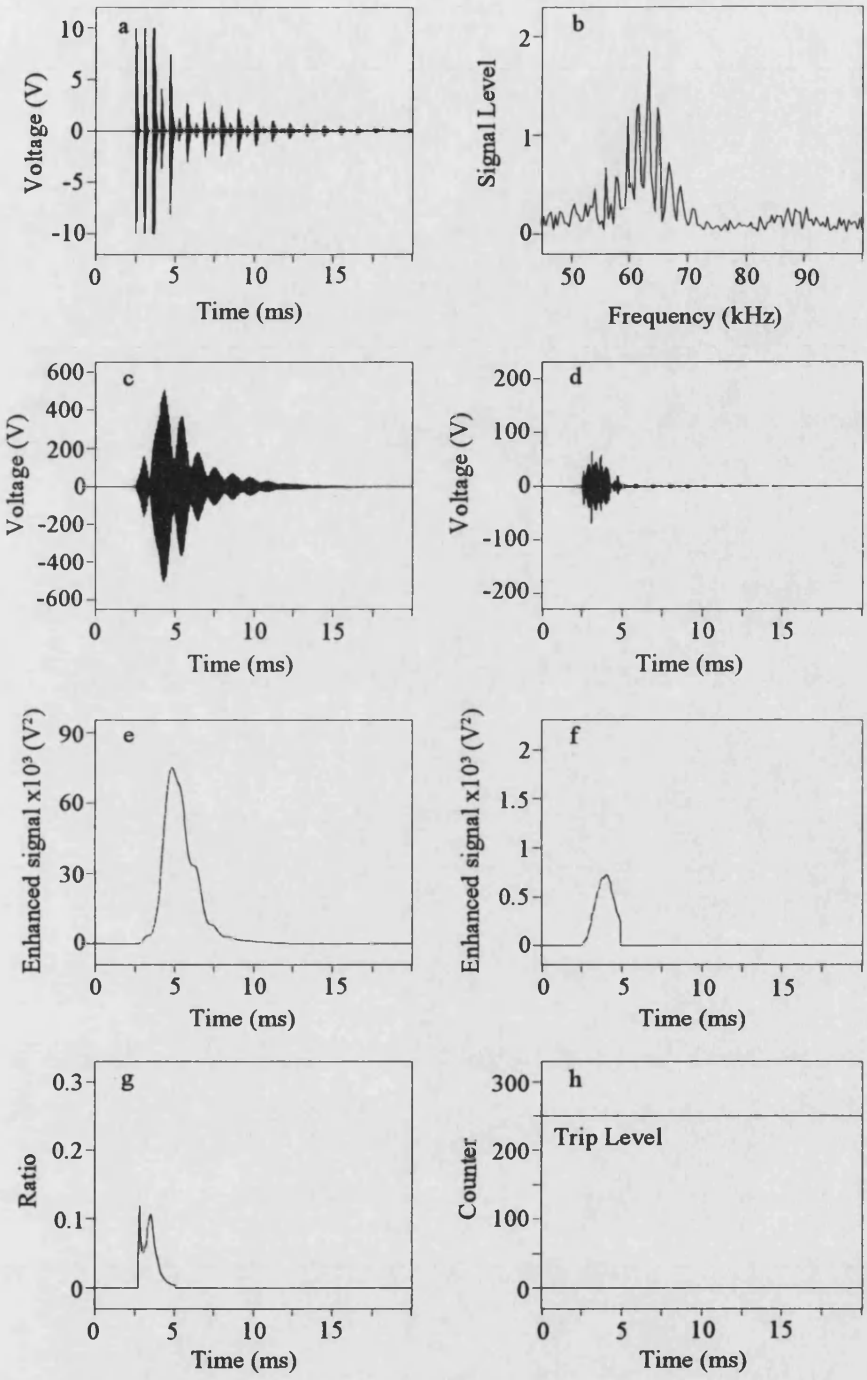
Fig. 6.23 - External 45° fault mode V_x response at end P



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

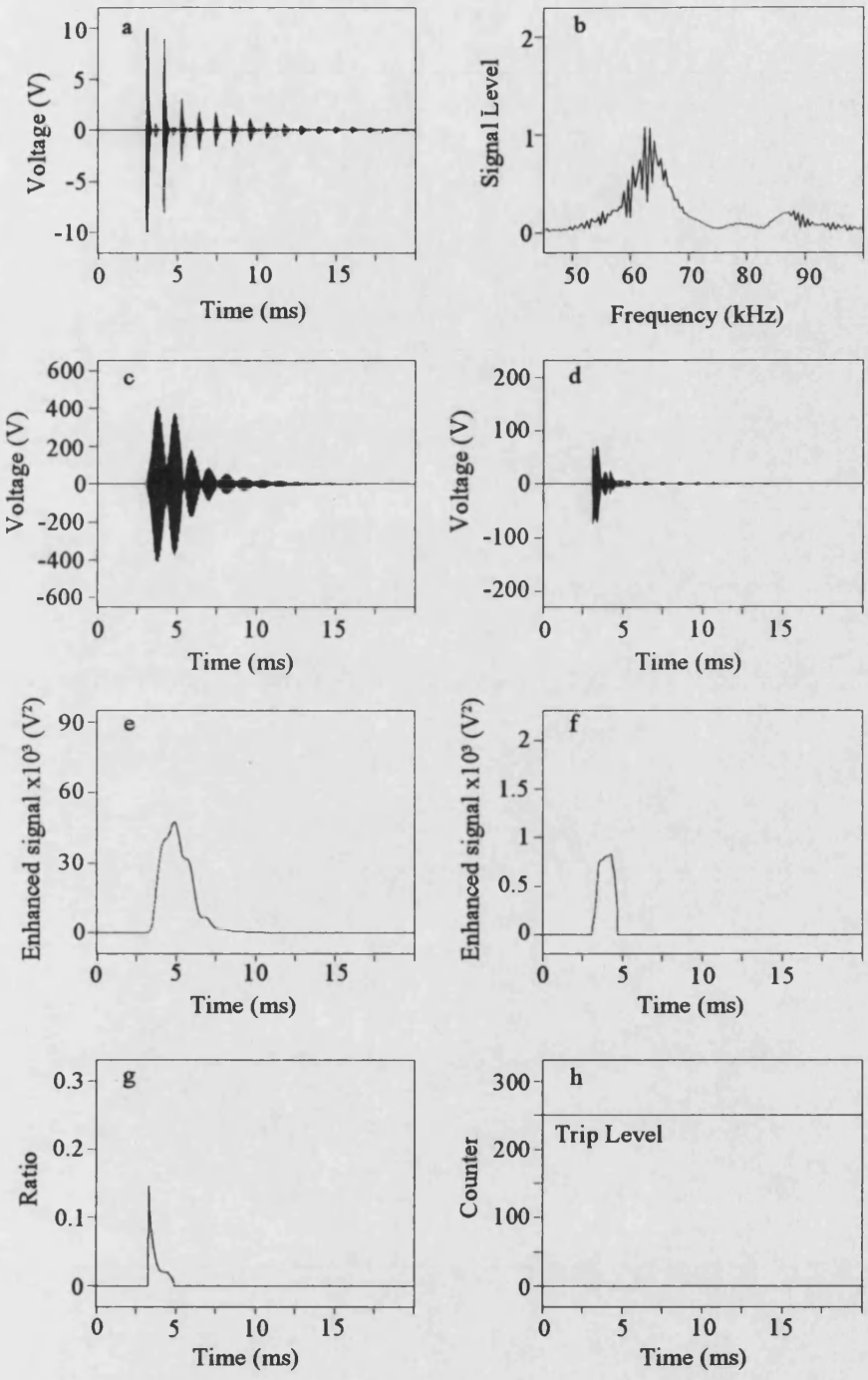
Fig. 6.24 - External 45° fault mode V_x response at end Q



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.25 - External 90° fault mode V_x response at end P



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.26 - External 90° fault mode V_x response at end Q

Table 6.3 shows the trip performance for the three external fault examples. All of the trip counters remain at zero and so a 'no trip' decision is correctly given in each case.

Table 6.3 - The effect of fault inception angle on trip times

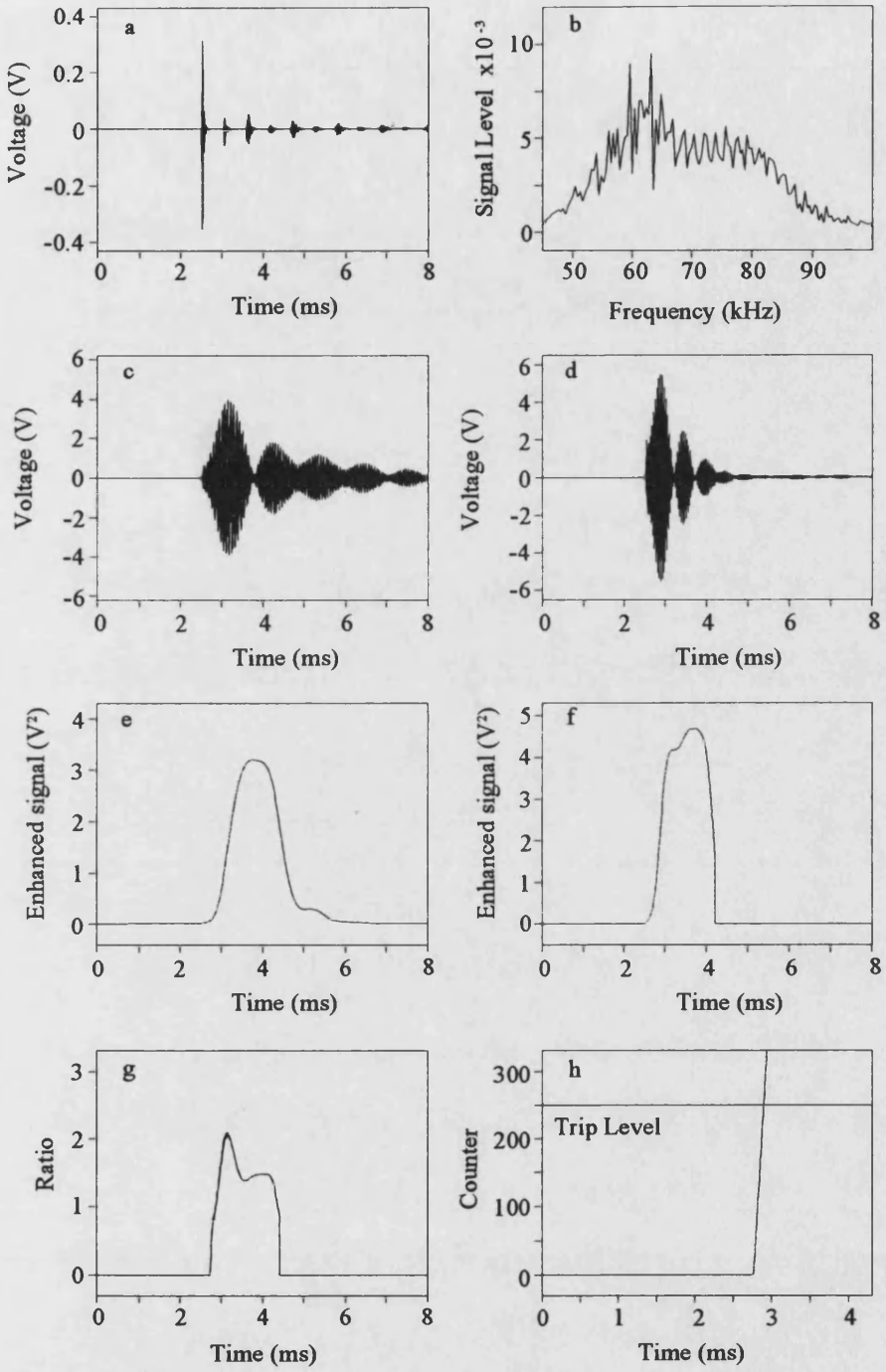
N/O - No Operation

Fault characteristics Note: Fault angle is the angle of V_a at end P			Time to trip after fault inception (ms)			
			End P		End Q	
Position	Angle	Type	Mode V_x	Mode V_y	Mode V_x	Mode V_y
F_2	0°	A-E	N/O	N/O	N/O	N/O
F_2	45°	A-E	N/O	N/O	N/O	N/O
F_2	90°	A-E	N/O	N/O	N/O	N/O

6.6 The Effect of Fault Position

The position of the fault has a distinct effect on the signals detected by the stack tuners. The most significant difference is whether the fault is internal or external to the protected zone. This was discussed in section 3.2 and is central to the correct operation of this protection method. The differences in the captured signals can be examined by comparing all of the mode V_x calculations at ends P and Q for three internal faults on the symmetrical tee network of Fig. 6.1a. They are all phase a to earth faults with a near zero fault inception angle and are applied at end P (F_1), 40 km from end P (F_5) and at the tee point (F_7).

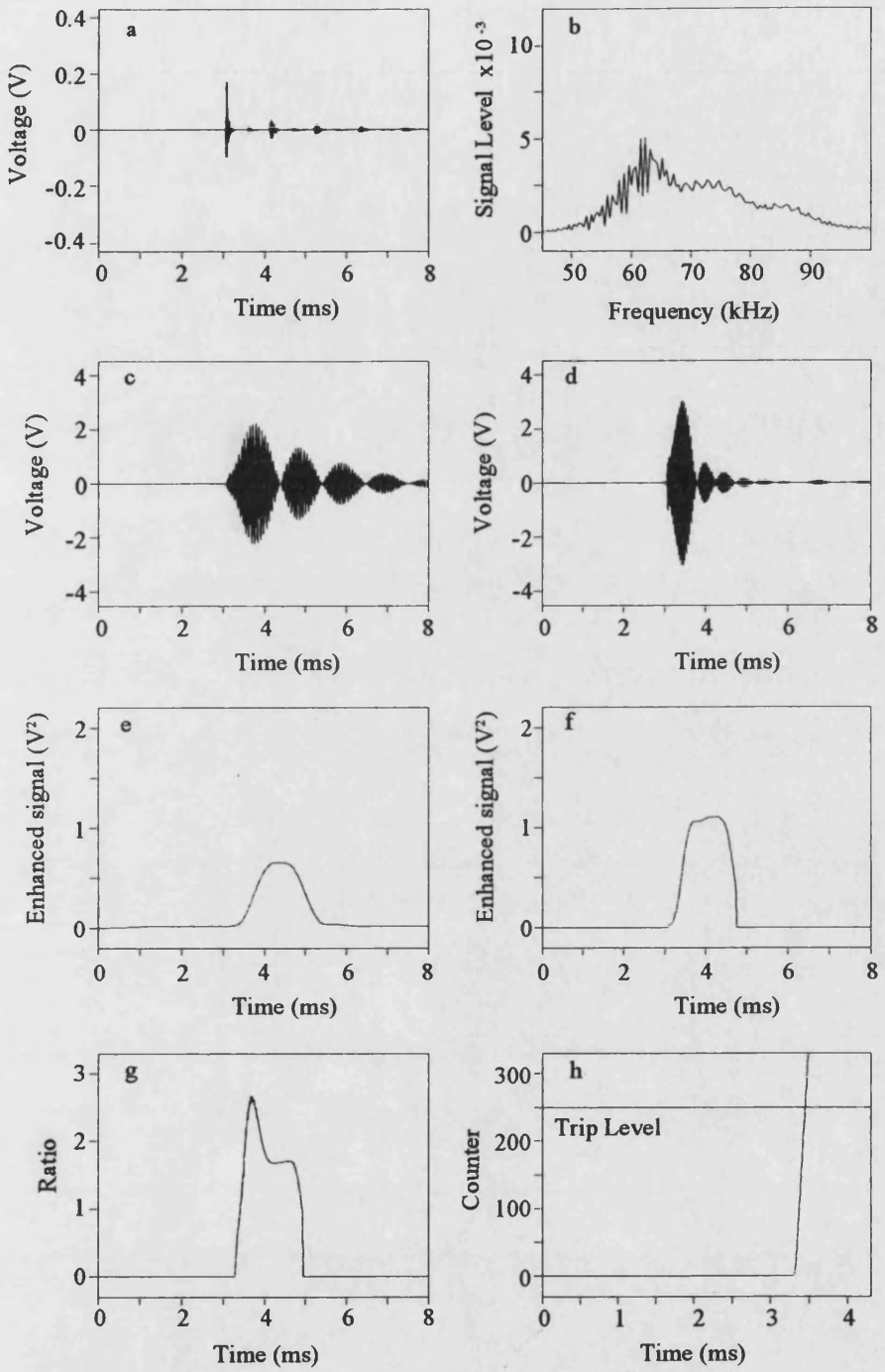
The waveforms for the fault at F_1 for ends P and Q are shown in Figs. 6.27 and 6.28. Figures 6.29 and 6.30 show the outputs at the two ends for the fault at F_5 and the F_7 fault case results are shown in Figs. 6.31 and 6.32.



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

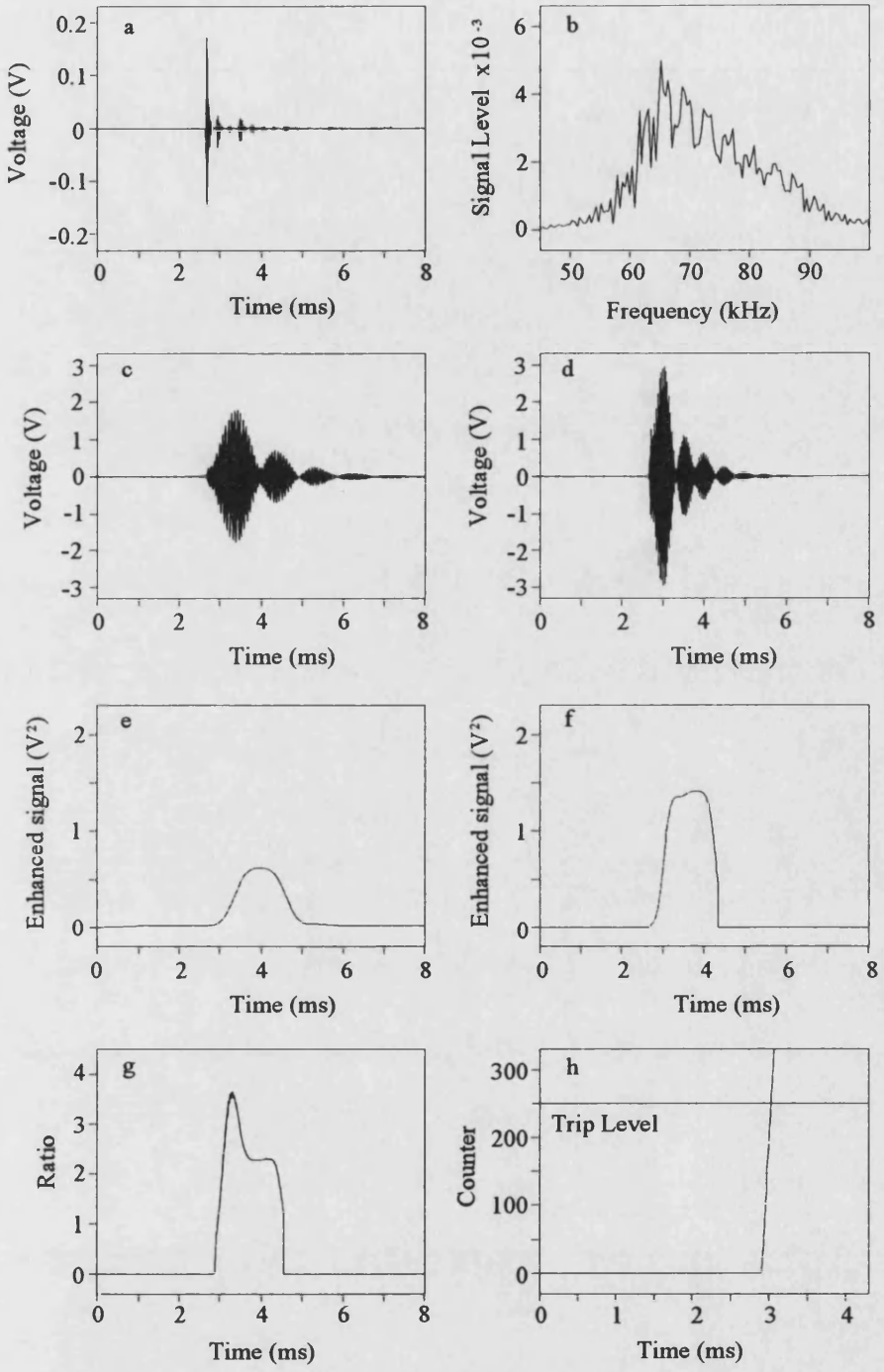
Fig. 6.27 - End P response for fault at F_1



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, t_f = 2.5 ms

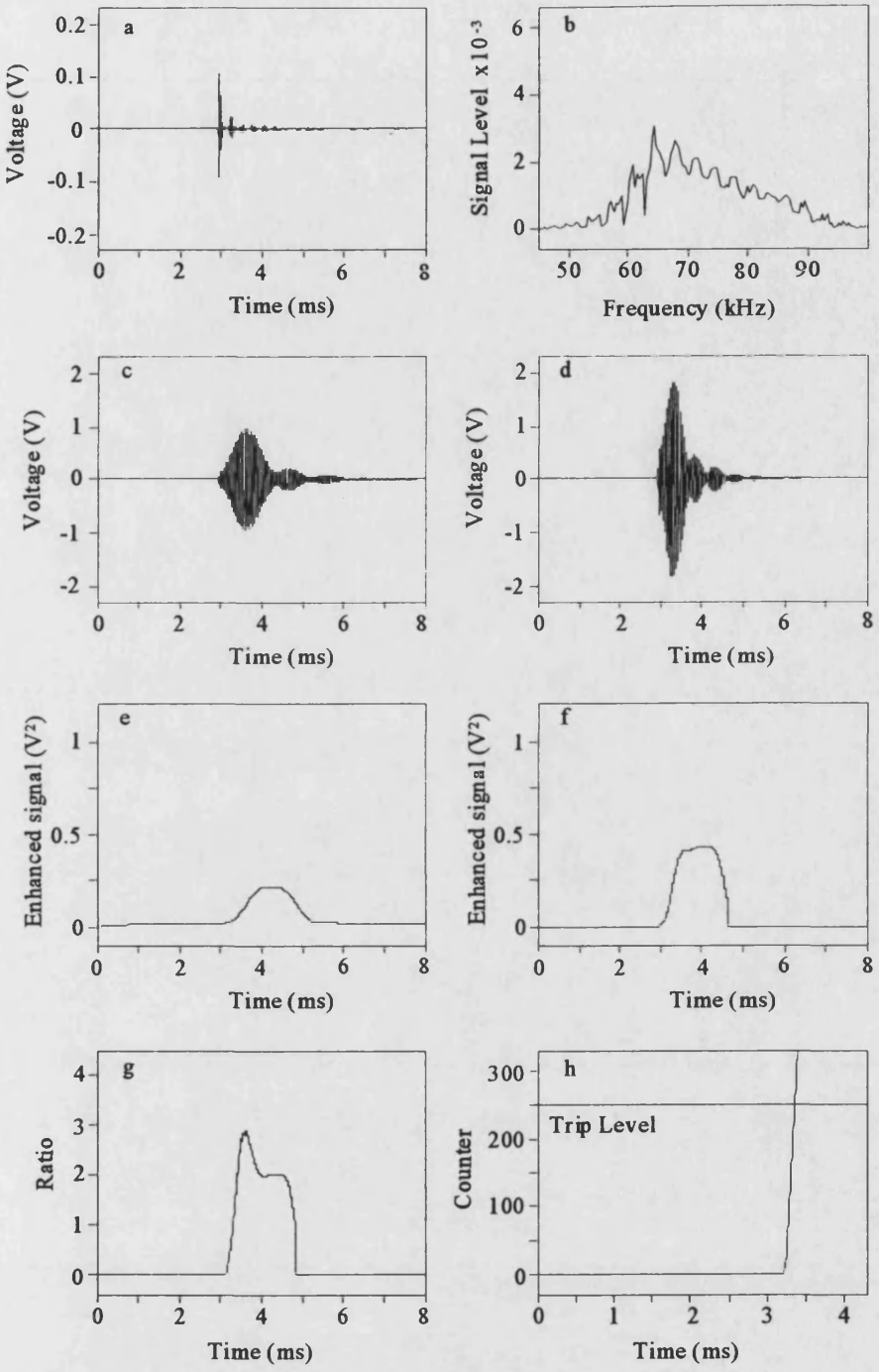
Fig. 6.28 - End Q response for fault at F_1



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

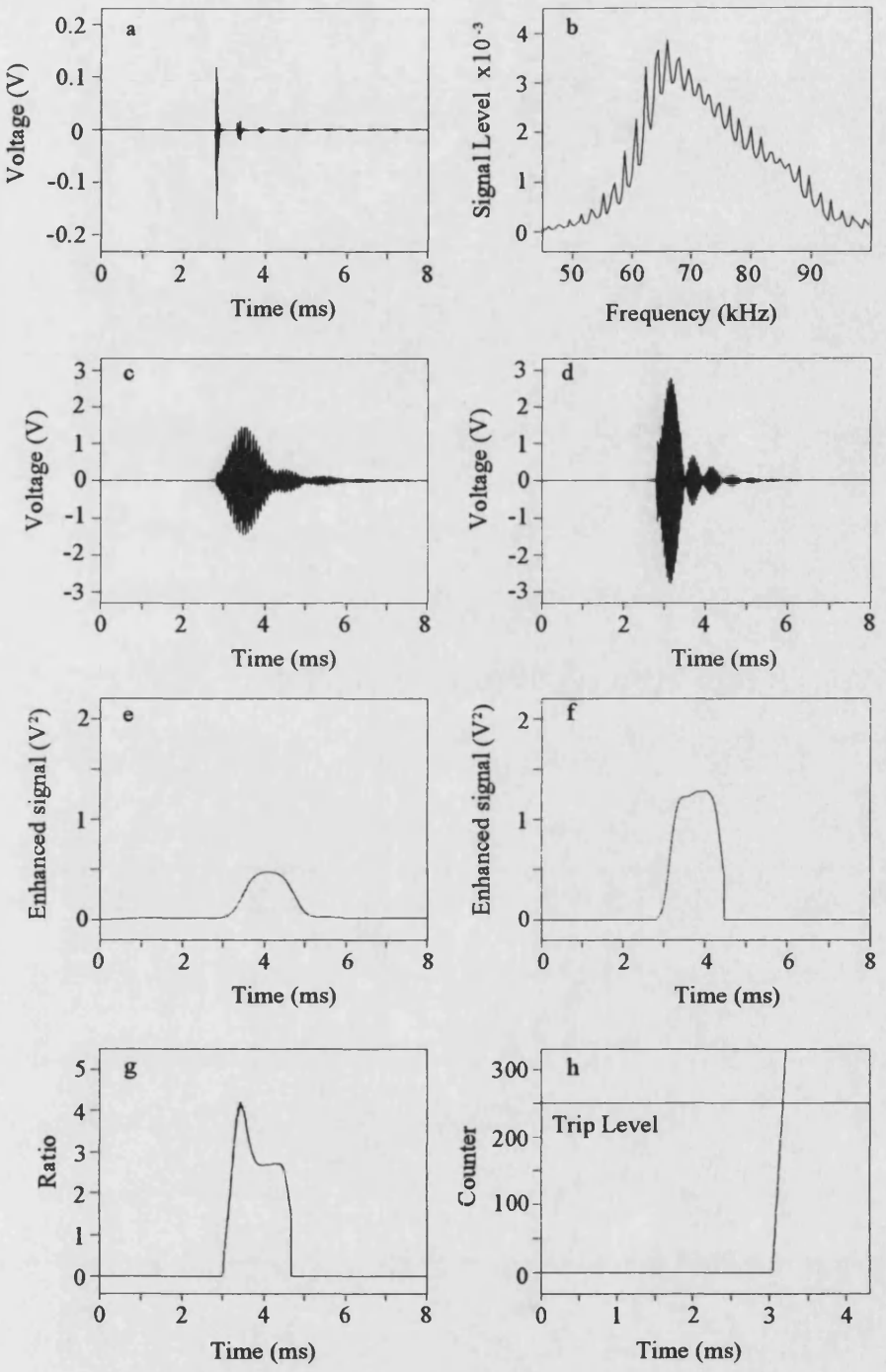
Fig. 6.29 - End P response for fault at F_5



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, t_f = 2.5 ms

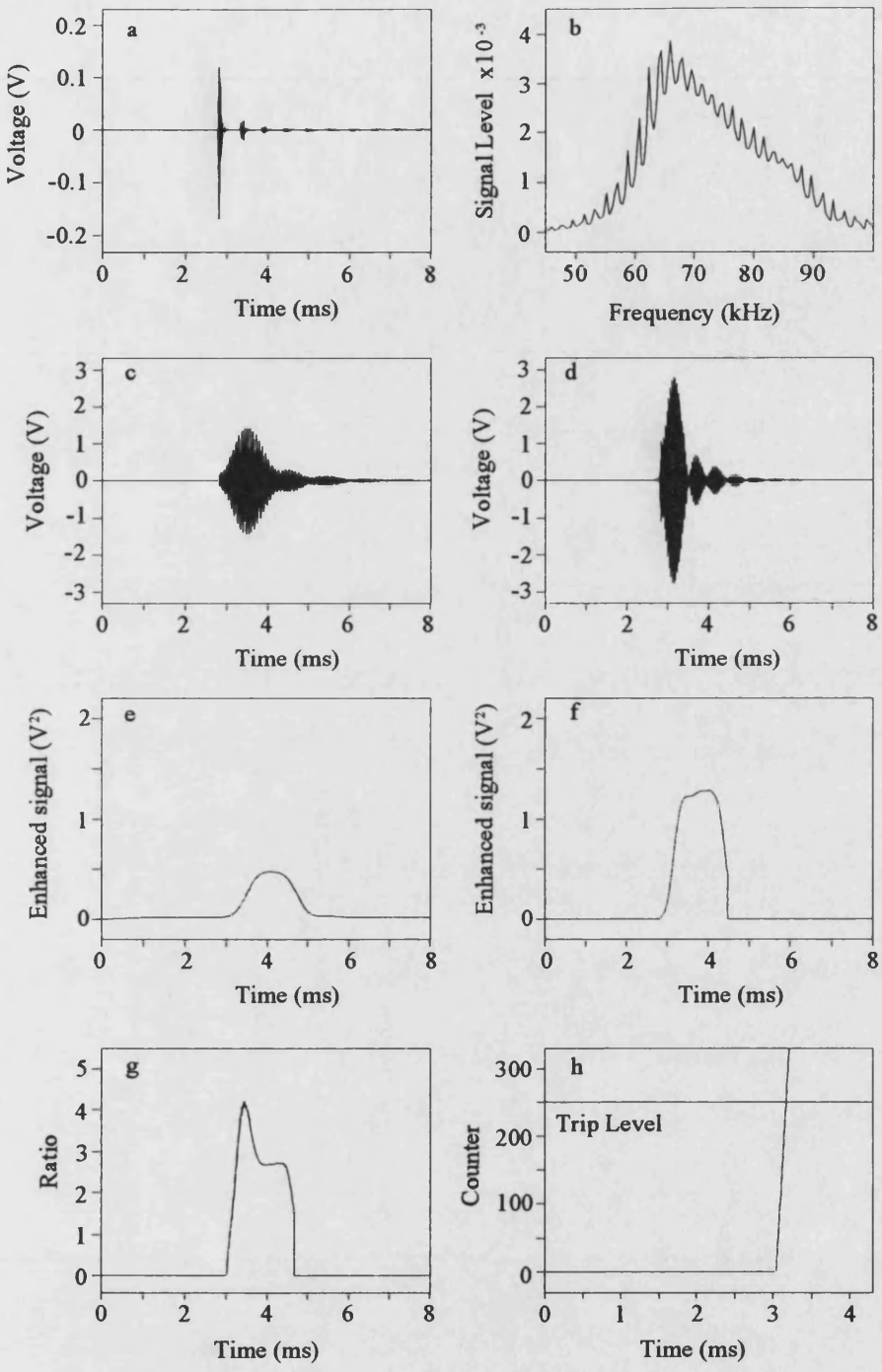
Fig. 6.30 - End Q response for fault at F_5



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.31 - End P response for fault at F_7



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

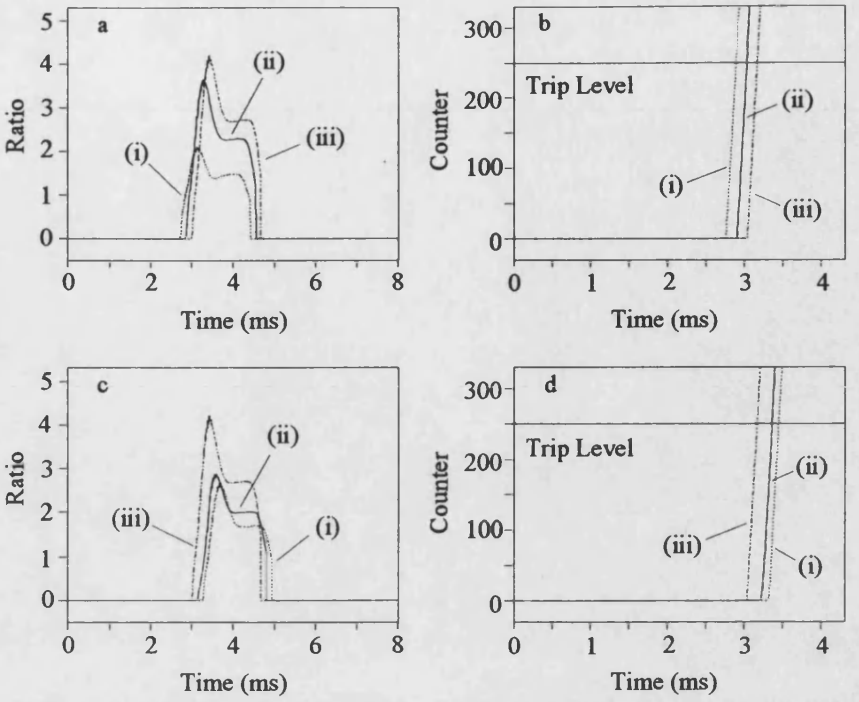
Fault inception, $t_f = 2.5$ ms

Fig. 6.32 - End Q response for fault at F_7

A number of trends are apparent from examining these fault responses. As the distance from the measurement point to the fault point increases, the magnitudes of the signals decreases and the time delay increases. This is due to the attenuation of the line and the presence of the tee point, and the finite propagation velocity of the transients, respectively.

Figure 6.33 shows a comparison of the discrimination ratios for the three faults, at ends P and Q, and their trip counter outputs. The discrimination ratios, and consequently the trip counter outputs, are primarily dependant on the time taken for the fault generated signals to reach the measurement points. This is because they are determined from the relative magnitudes of components of the captured signals and not on their actual magnitudes.

The trip times for both modes are shown in Table 6.4. There is little difference in the performance of the two modes, with a trip decision being issued less than one millisecond after fault inception. The results are identical at ends P and Q for the fault at the tee point, due to the symmetry of the network.



a End P discrimination ratios b End P trip counter outputs (i) Fault at F_1
c End Q discrimination ratios d End Q trip counter outputs (ii) Fault at F_5
Fault inception, $t_f = 2.5$ ms (iii) Fault at F_7

Fig. 6.33 - Effect of fault position on performance

Table 6.4 - The effect of fault position on trip times

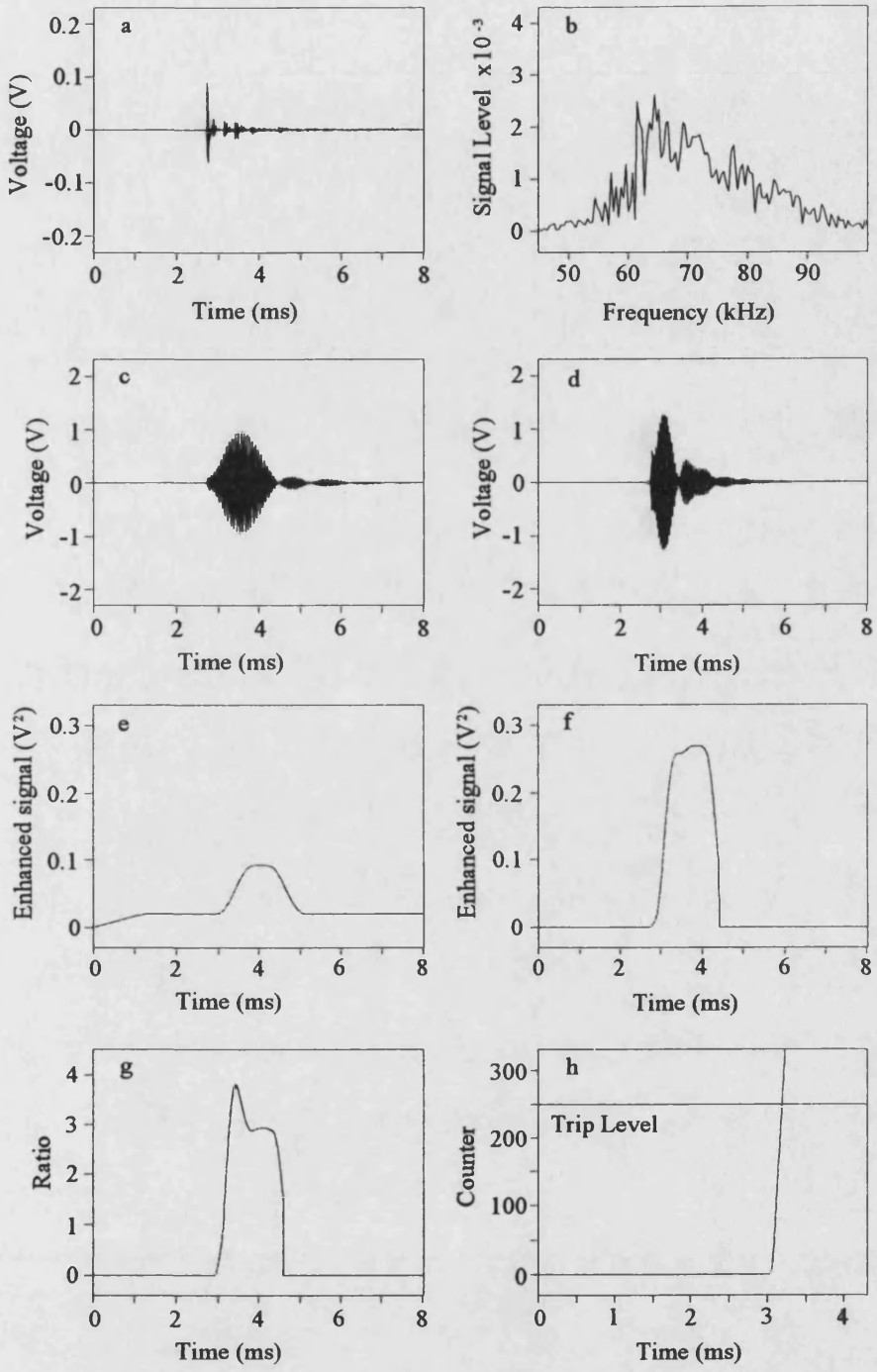
Fault characteristics Note: Fault angle is the angle of V_a at end P			Time to trip after fault inception (ms)			
			End P		End Q	
Position	Angle	Type	Mode V_x	Mode V_y	Mode V_x	Mode V_y
F_1	0°	A-E	0.395	0.385	0.950	0.990
F_5	0°	A-E	0.530	0.555	0.860	0.890
F_7	0°	A-E	0.670	0.685	0.670	0.685

6.7 The Effect of Fault Type

This section examines the effect of different fault types on the waveforms that are derived from the captured signals. The single phase to earth fault and the phase to phase clear of earth fault are applied at point on wave where there is minimum voltage disturbance. For the single phase to earth fault this is simply when the phase voltage of the relevant phase is at zero. The phase to phase fault is applied when the voltage magnitudes of the two phases are equal. The phase to phase to earth fault is again applied when the voltage magnitudes of the phases are equal. The three phase fault clear of earth and the three phase to earth fault are both applied when the phase a voltage is equal to zero. All of the faults are applied 60 km from end P on the symmetrical tee network at point F_6 in Fig. 6.1a.

6.7.1 Single Phase to Earth Faults

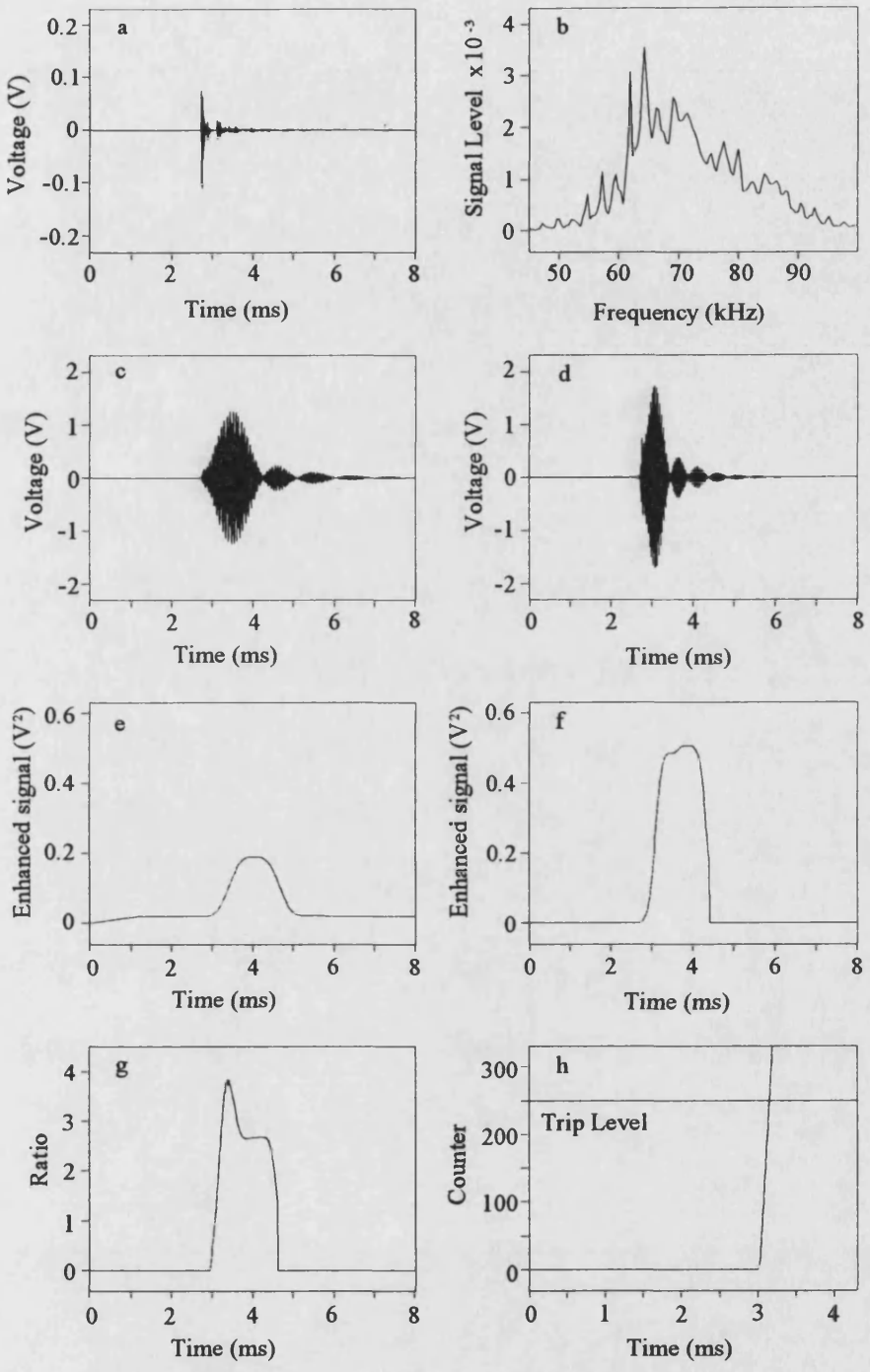
A large number of phase a to earth faults have already been studied extensively in this thesis. Figures 6.34 and 6.35 show the mode V_x and V_y waveforms at end P for a phase c to earth fault. This demonstrates that there are no significant differences between the single phase to earth faults. The frequency spectra of the two modes show a slight variation which is due to the different phase voltage combinations that are used to determine the modes. It should also be noted that mode V_y does not cover phase b to earth faults.



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.34 - A-E fault mode V_x response at end P



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

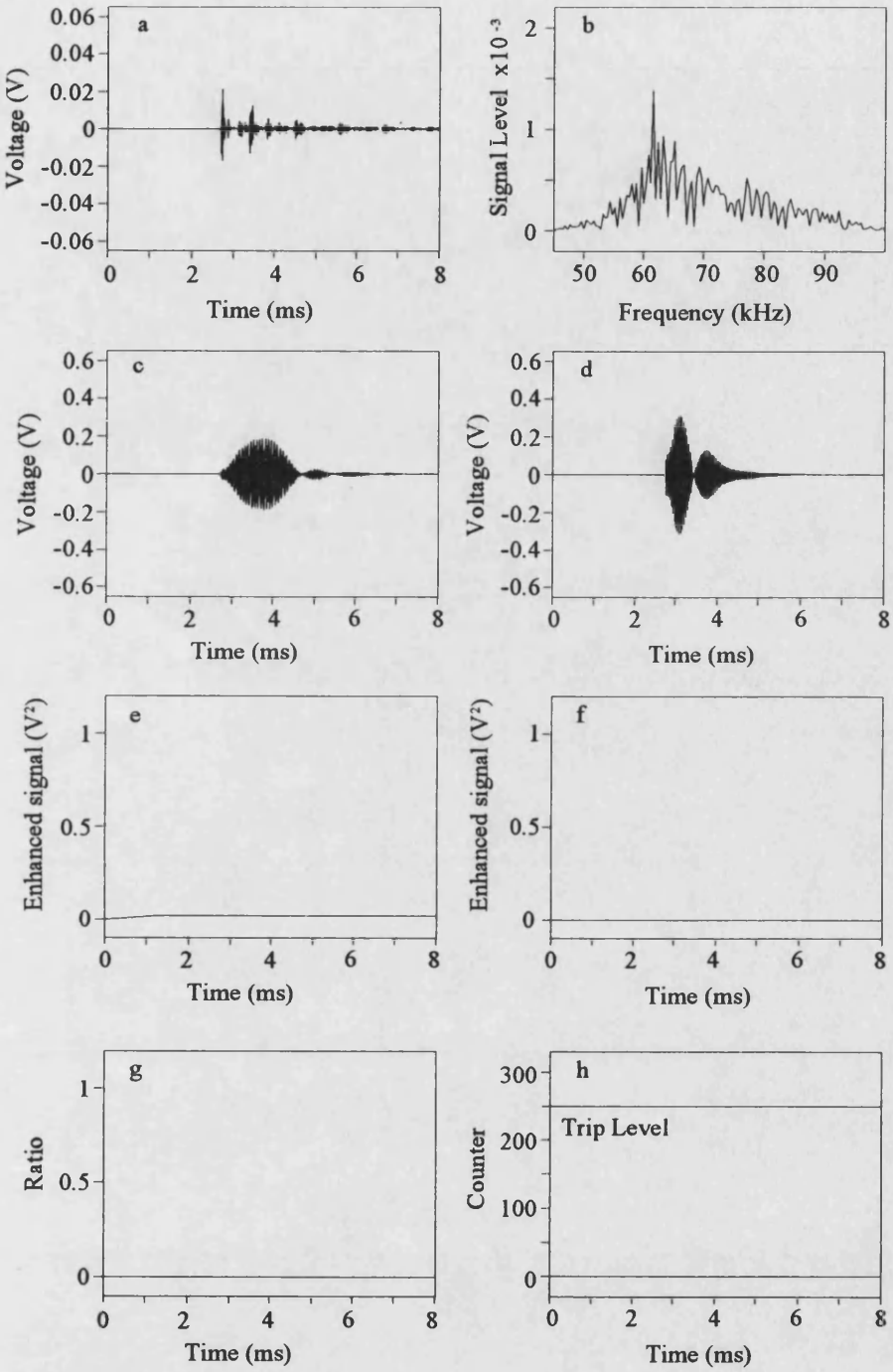
Fault inception, $t_f = 2.5$ ms

Fig. 6.35 - A-E fault mode V_y response at end P

6.7.2 Phase to Phase Faults

Phase a to phase c faults clear of earth are not covered by mode V_x and this can be seen clearly in Fig. 6.36. Only a small amount of HF signals are captured because of the voltage composition of mode V_x (Fig. 6.36a). The filter outputs are therefore very small (Figs. 6.36c,d) and are reduced further by the enhancement process as they are less than one. They fall below the minimum threshold set within the algorithm and so the enhanced restraint filter output is forced to 0.02 and the enhanced operate filter is forced to zero (Figs. 6.36e,f). The discrimination ratio, therefore, stays at zero and no trip decision is issued. Mode V_y has been included to cover this specific fault condition and correctly gives a trip output at end P about 0.6 ms after fault inception (Fig. 6.37).

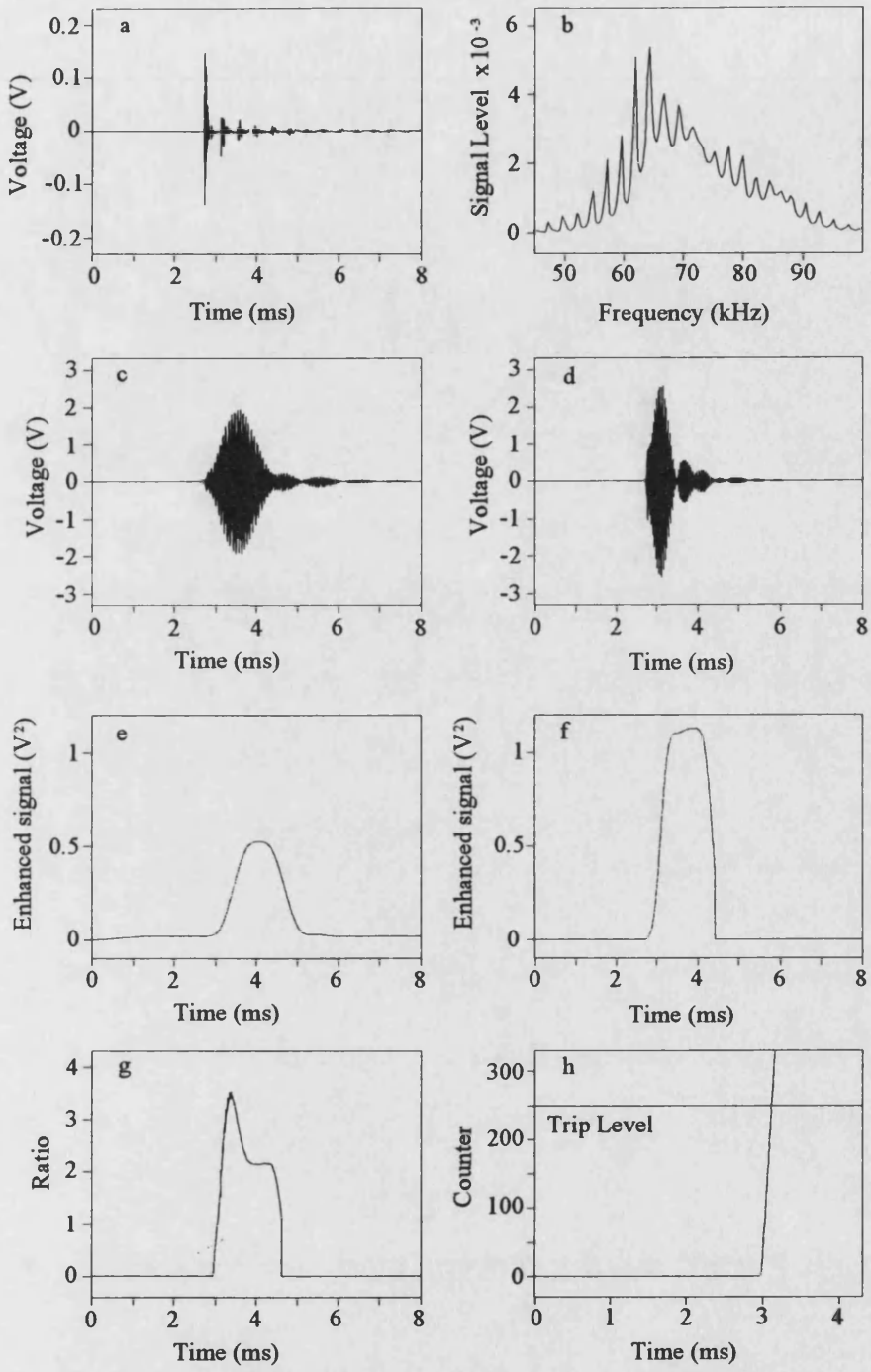
Faults involving more than one phase produce larger amounts of HF components as the energy of each of the phases is released. There is also potential for larger disturbances as the line to line voltage has a larger magnitude than the phase to earth voltage, but this will depend on the fault inception angle relative to the phases concerned.



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.36 - A-C fault mode V_x response at end P



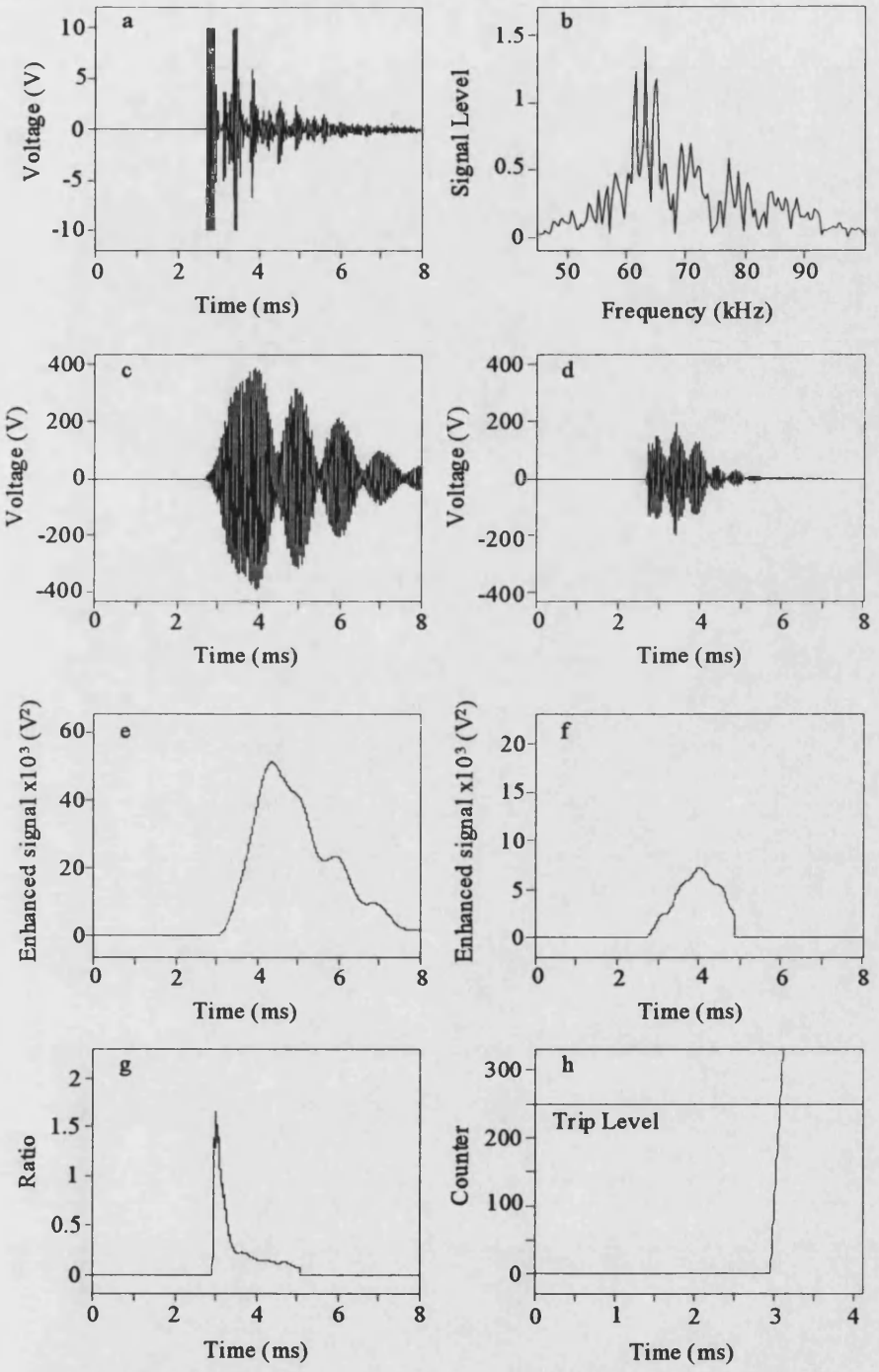
a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.37 - A-C fault mode V_y response at end P

6.7.3 Phase to Phase to Earth Faults

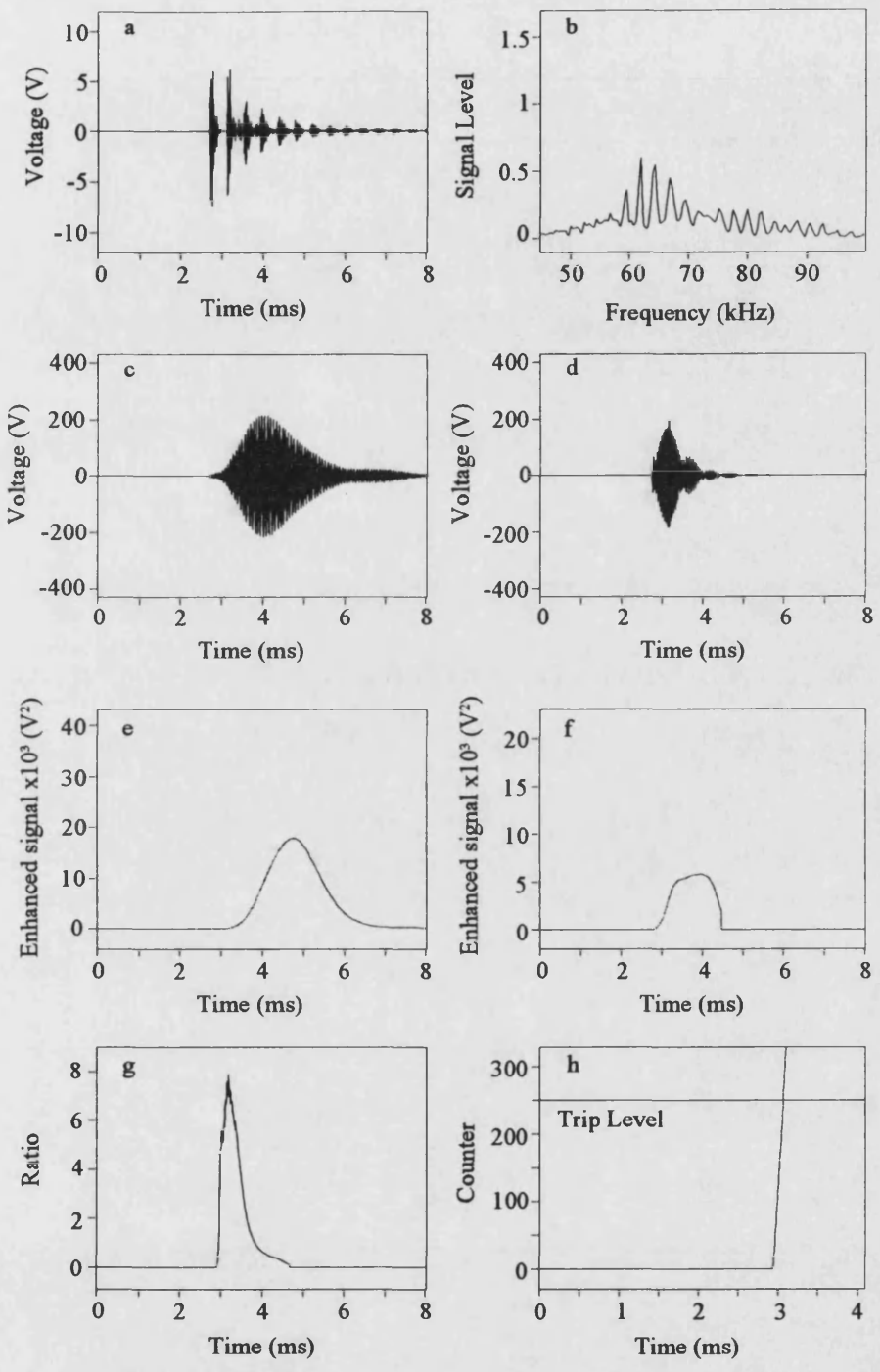
A phase a to phase c to earth fault is applied when the two phase voltage magnitudes are equal. Considerably larger quantities of HF signals are detected in this case because both phase voltages are reduced to earth potential (Figs. 6.38, 6.39). The very large enhanced filter outputs are partly due to the effect of the moving average algorithm (Figs. 6.38e,f, 6.39e,f). The 250 sample long window means that the energy from a number of bursts are accumulated to give the high outputs. It should also be noted that the discrimination ratios peak at approximately 3 ms whereas the enhanced filter outputs peak after 4 ms (Figs. 6.38g, 6.39g). This shows that the trip decision is principally made using the information from the initial burst of signals. Both modes give trip decisions just under 0.6 ms after fault inception.



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, t_f = 2.5 ms

Fig. 6.38 - A-C-E fault mode V_x response at end P



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, t_f = 2.5 ms

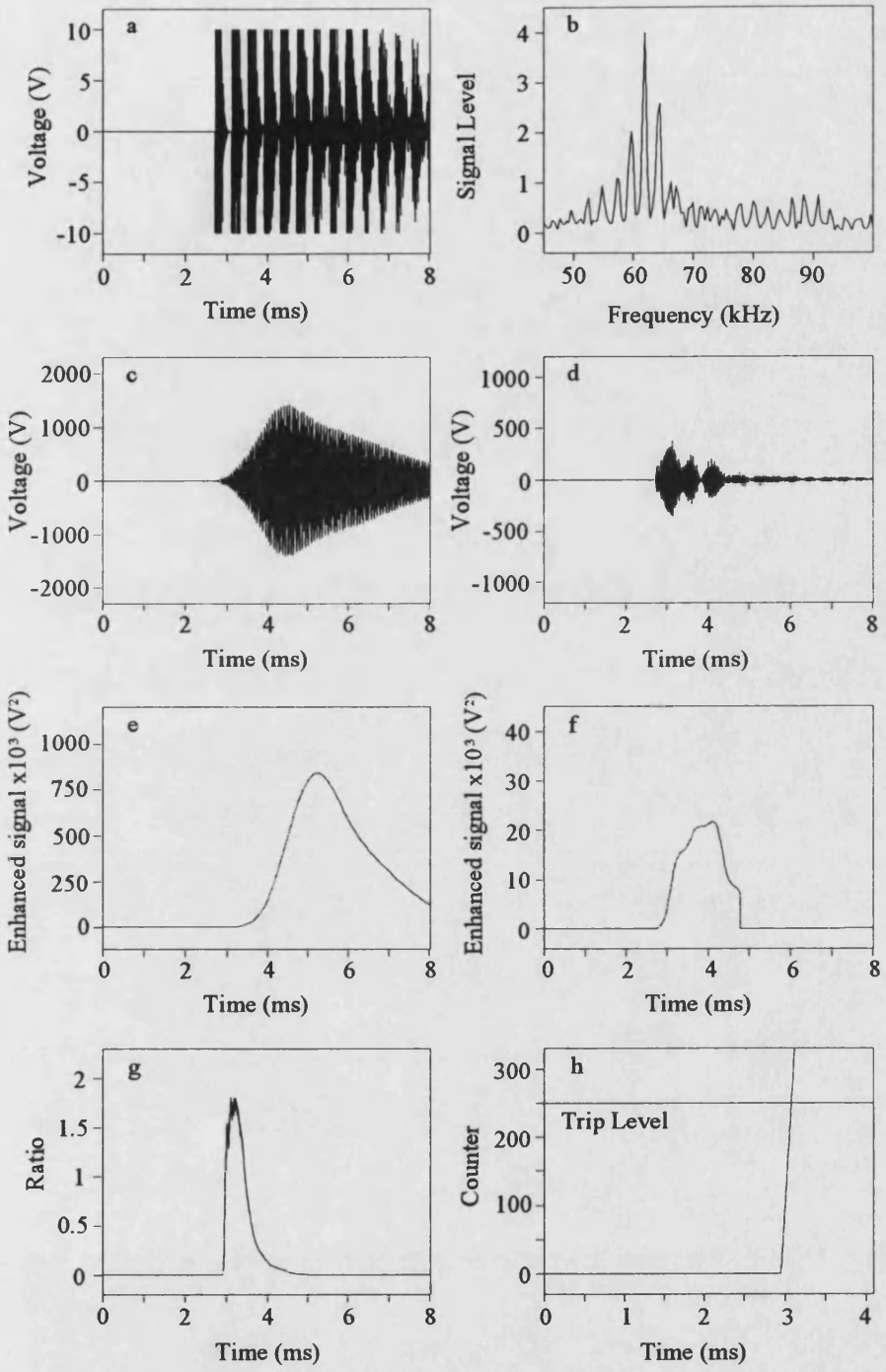
Fig. 6.39 - A-C-E fault mode V_y response at end P

6.7.4 Three Phase Faults

Three phase faults are the most severe type encountered on a power system whether they are clear of earth or not. The considerable energy of the initial bursts can clearly be seen in Figs. 6.40 and 6.41, particularly in the V_x mode. Many of the subsequent reflections also have to be clipped and the frequency spectrum shows substantial amounts of energy around 60 kHz (Figs. 6.40a,b).

The enhanced filter outputs reach very high values as the components of the individual reflections are averaged together (Figs. 6.40e,f). The trip decision is again reached at end P after approximately 0.6 ms, which is before the enhanced filter outputs reach their maximum values.

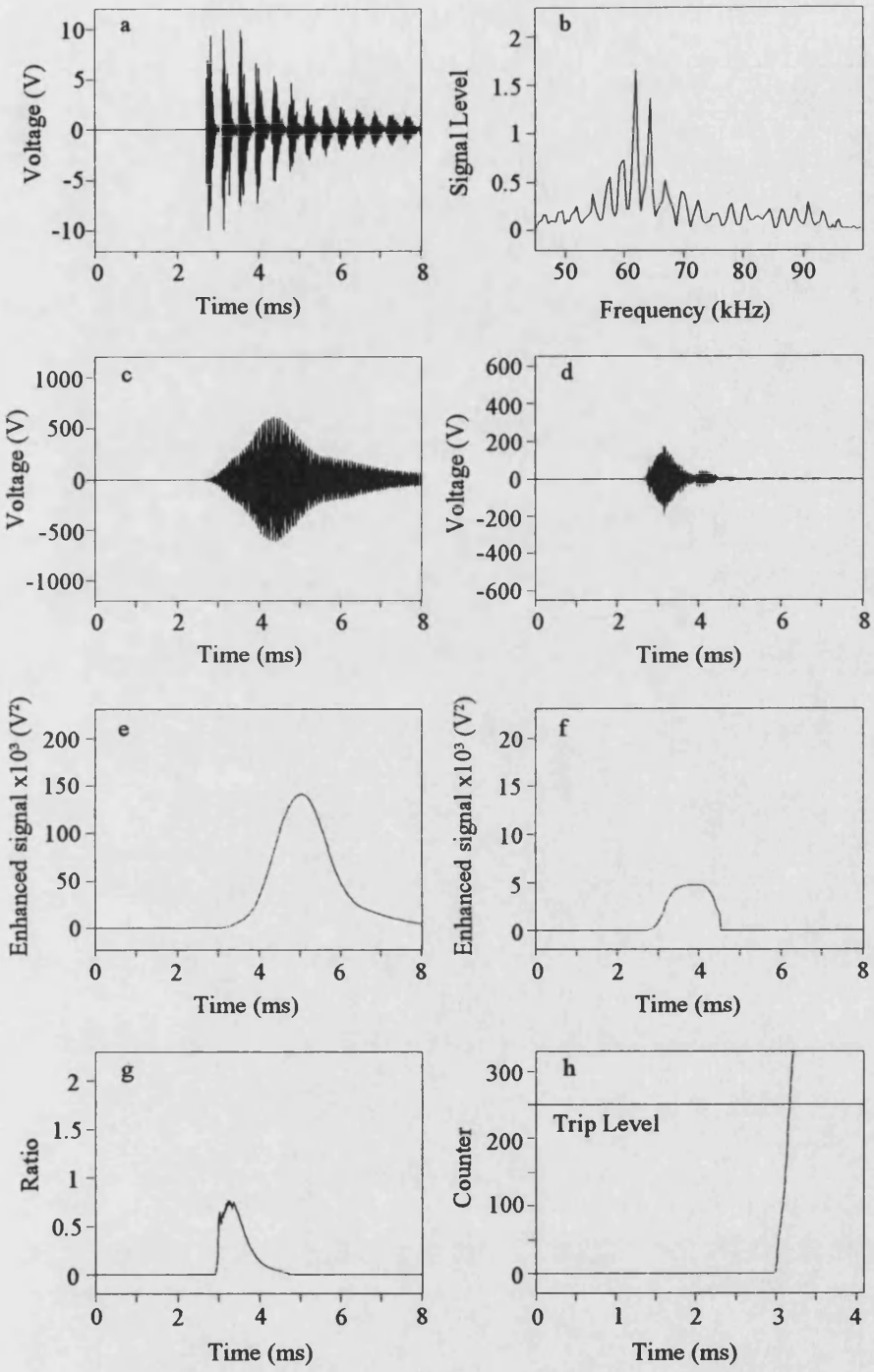
The signals detected by mode V_y are lower than for mode V_x as a direct result of their modal voltage composition (Fig. 6.41a). The components extracted from the individual bursts are again combined by the moving average process and a trip decision is given in just under 0.7 ms.



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.40 - A-B-C fault mode V_x response at end P



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.41 - A-B-C fault mode V_y response at end P

6.7.5 Three Phase to Earth Faults

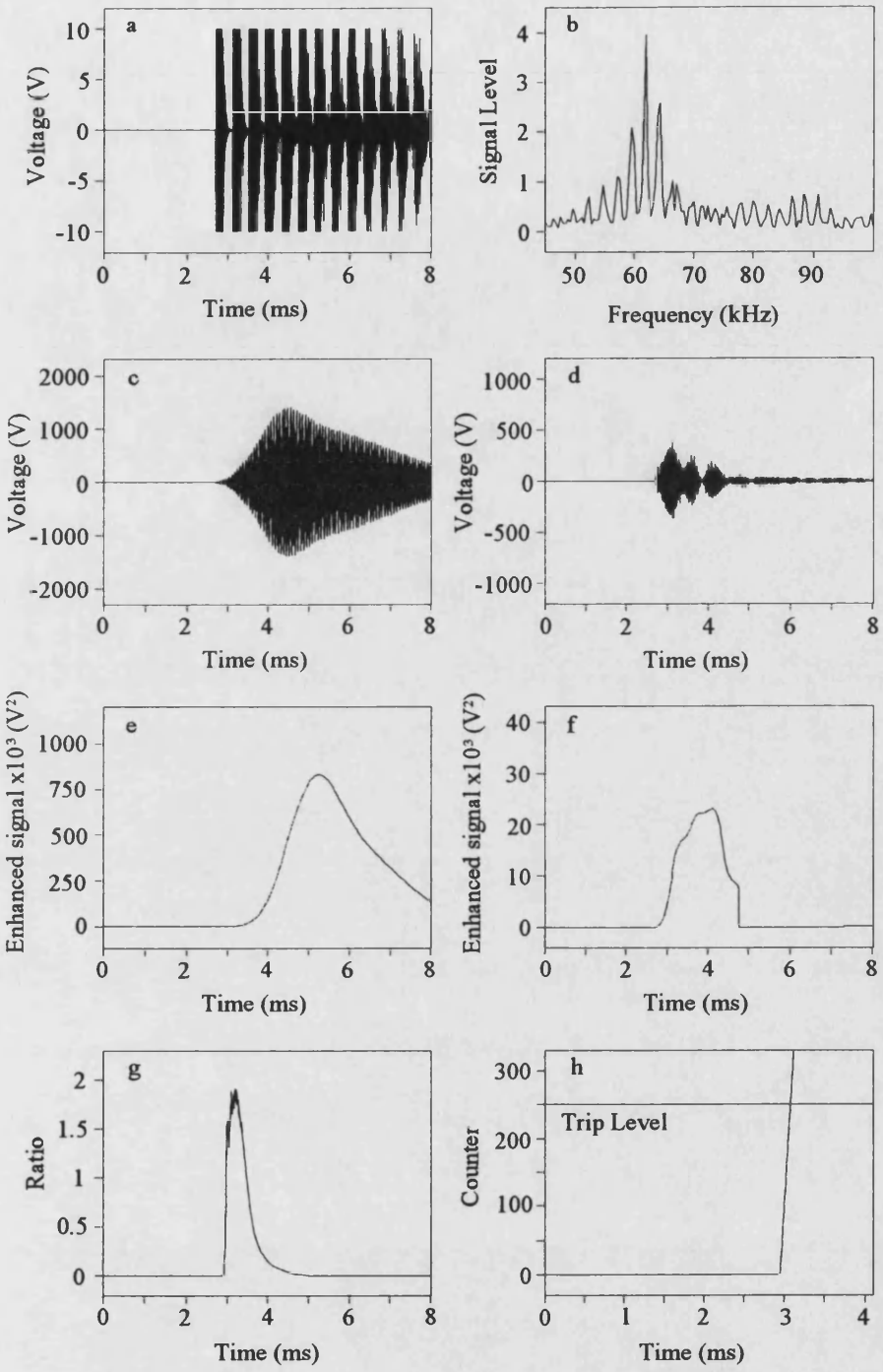
There are no major differences between the waveforms for a three phase fault and a three phase to earth fault (Figs. 6.42, 6.43). Very large enhanced outputs are again recorded and trip decision are given in approximately 0.6 ms and 0.7 ms for modes V_x and V_y respectively at end Q.

Table 6.5 shows the trip times for all of the fault types discussed in this section. The longer trip times at end Q are due to the greater distance of the fault point from that end. There is no distinct trend in the trip times associated with the type of fault and the trip decisions are all made less that one millisecond after fault inception.

Table 6.5 - The effect of fault type on trip times

N/O - No Operation

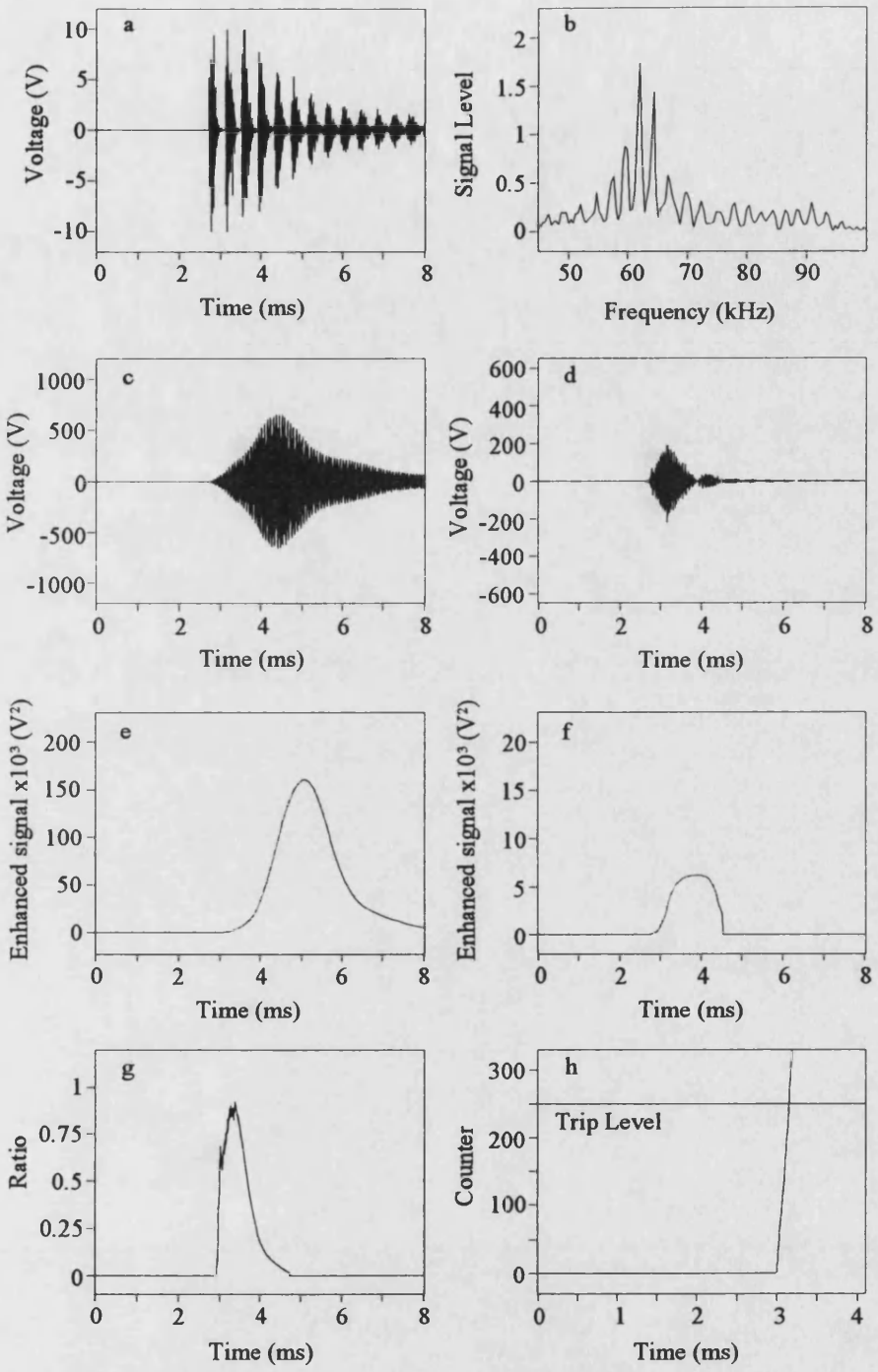
Fault characteristics Note: Fault angle is the angle of V_a at end P			Time to trip after fault inception (ms)			
			End P		End Q	
Position	Angle	Type	Mode V_x	Mode V_y	Mode V_x	Mode V_y
F_6	0°	C-E	0.690	0.650	0.945	0.890
F_6	75°	A-C	N/O	0.615	N/O	0.810
F_6	75°	A-C-E	0.575	0.565	0.705	0.705
F_6	0°	A-B-C	0.580	0.680	0.705	0.725
F_6	0°	A-B-C-E	0.575	0.650	0.705	0.720



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, t_f = 2.5 ms

Fig. 6.42 - A-B-C-E fault mode V_x response at end P



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

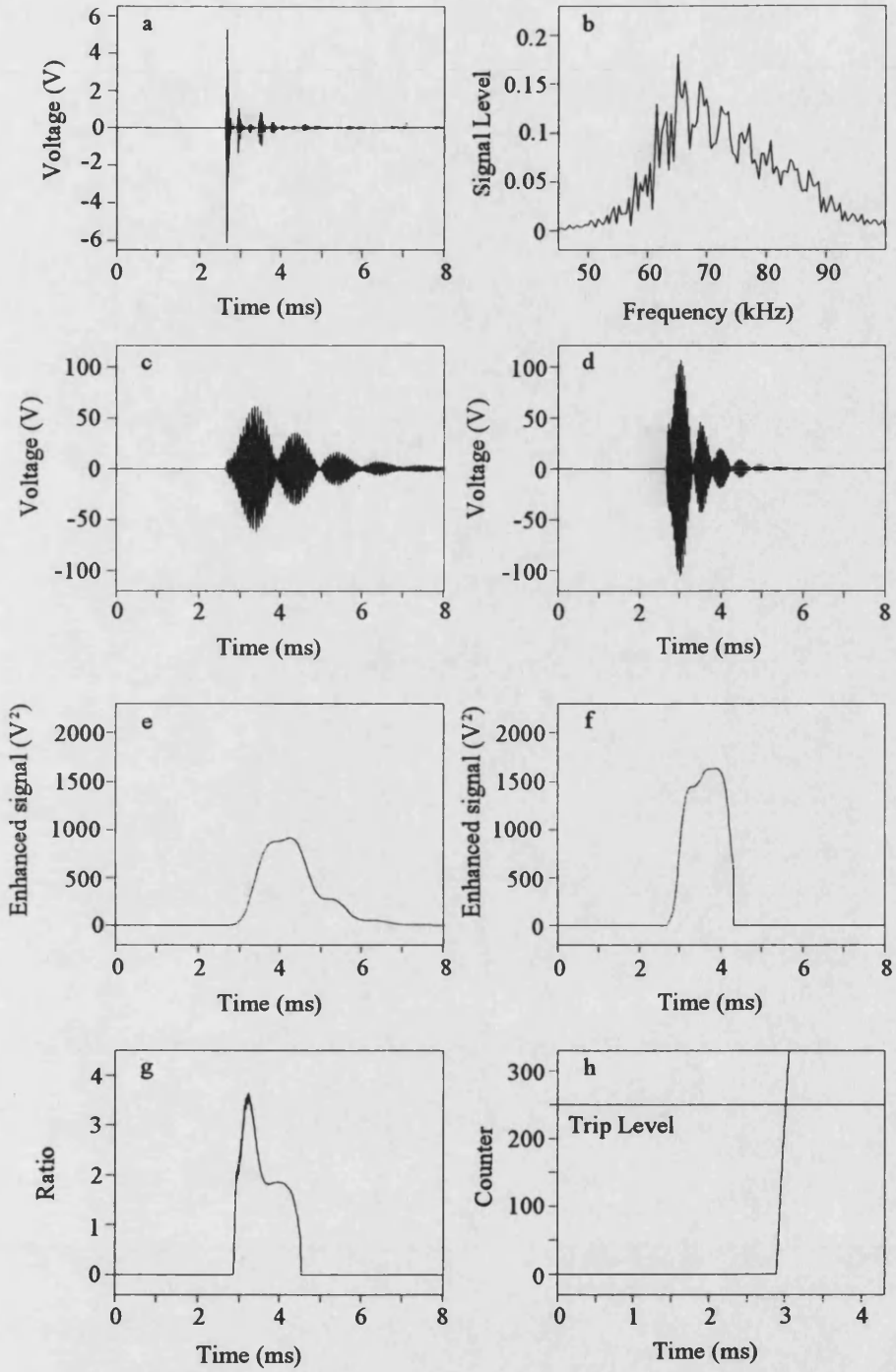
Fault inception, $t_f = 2.5$ ms

Fig. 6.43 - A-B-C-E fault mode V_y response at end P

6.8 Fault Resistance Effects

A series resistance was added to the arc resistance in the power system simulations to study the behaviour of the scheme to different fault resistances. A 5° phase a to earth fault was applied 40 km from end P on the symmetrical tee network (F_5 in Fig. 6.1a). The series resistance was set at 50 Ω, 100 Ω, 200 Ω and 300 Ω, as this covers the range of values that is likely to be encountered in practice.

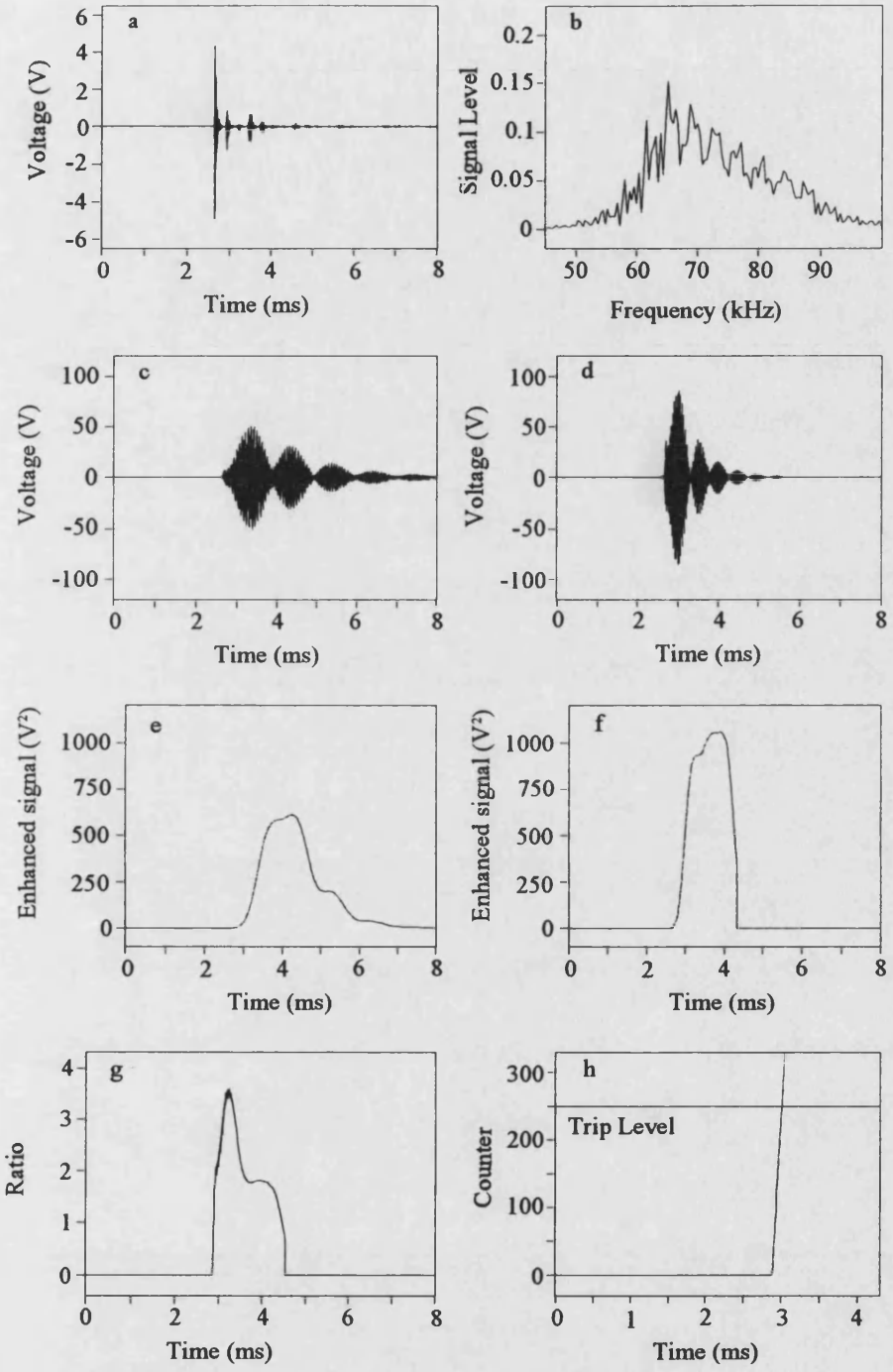
The waveforms of mode V_x at end P are shown in Figs. 6.44-6.47. These demonstrate that as the fault resistance is increased, the magnitude of the signals is reduced by the additional damping of the fault path.



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

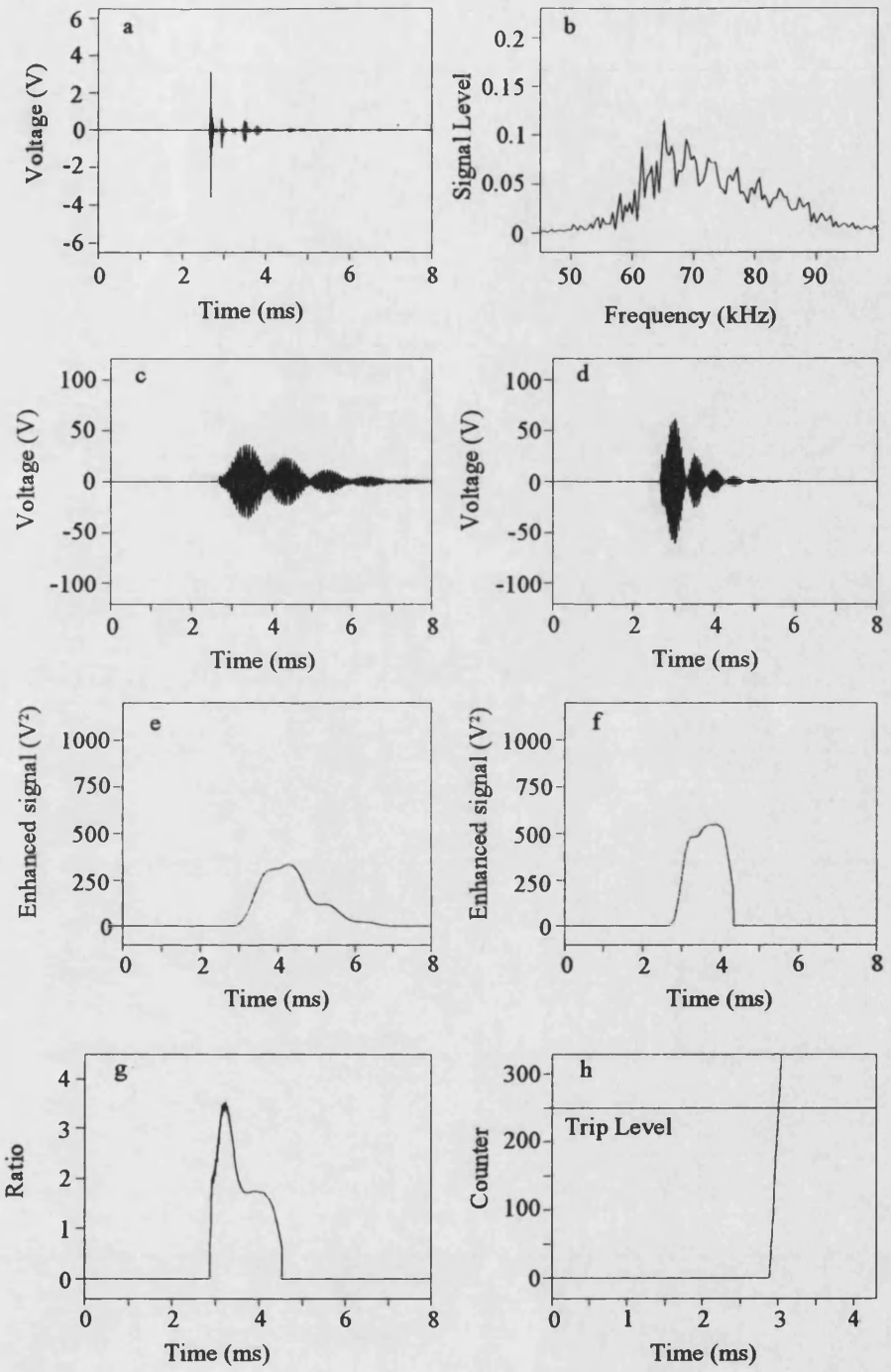
Fig. 6.44 - 50 Ω fault resistance mode V_x response at end P



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

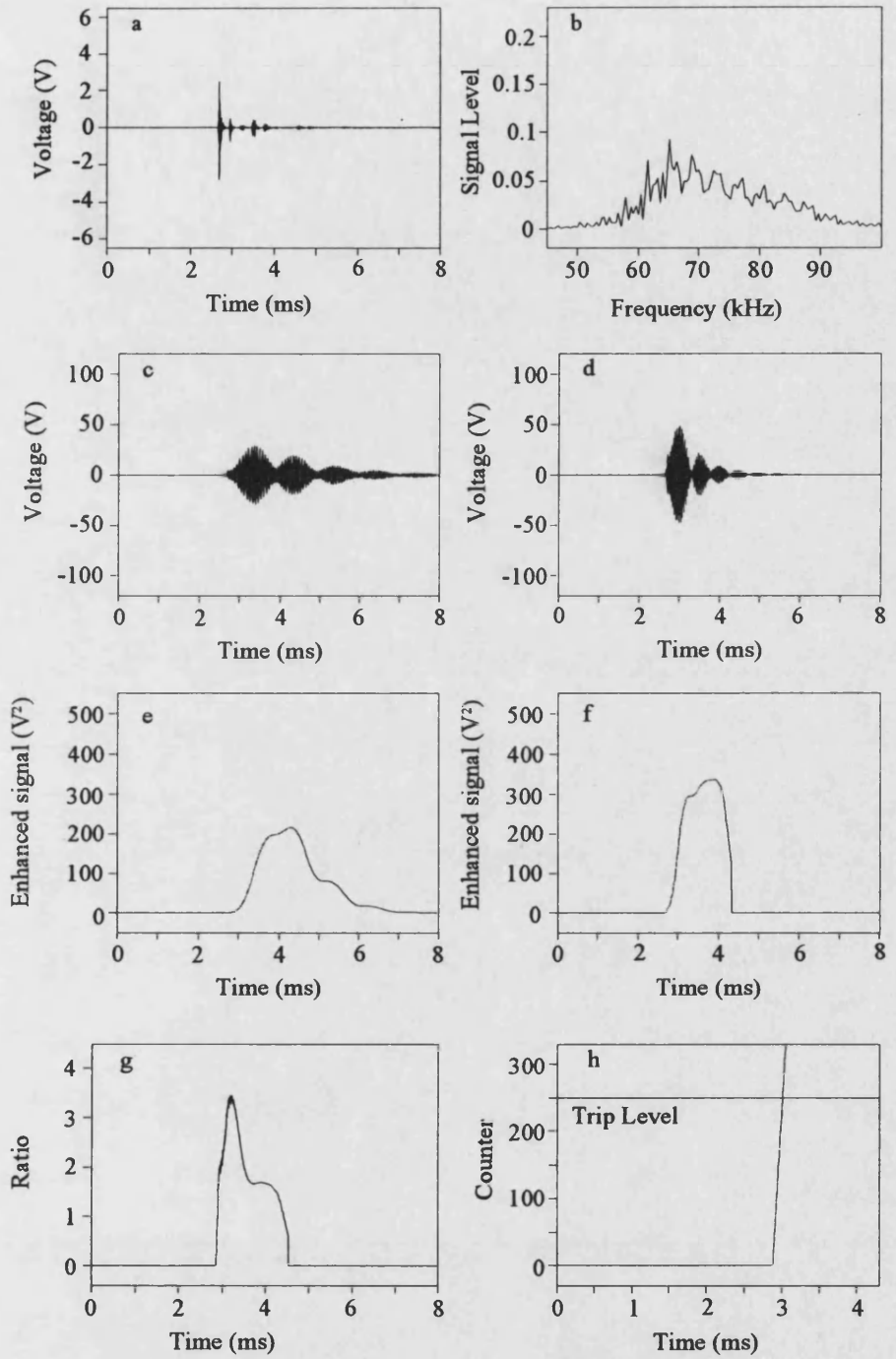
Fig. 6.45 - 100 Ω fault resistance mode V_x response at end P



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, t_f = 2.5 ms

Fig. 6.46 - 200 Ω fault resistance mode V_x response at end P



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.47 - 300 Ω fault resistance mode V_x response at end P

This reduction in the signal strength does not have any significant effect on the behaviour of the technique as can be seen in Fig. 6.48. There is hardly any difference in the discrimination ratios recorded at ends P and Q as it is calculated using a comparison of the amount of energy in the specific frequency bands and not their actual magnitudes. (End R signals are identical to end Q signals due to the symmetry of the network and so are not shown). This technique will start to become affected when the signal magnitudes are reduced down to the background noise level and the minimum threshold of the algorithm. This will be a function of the fault position, type and inception angle as this will determine the amount of HF signals that are generated initially.

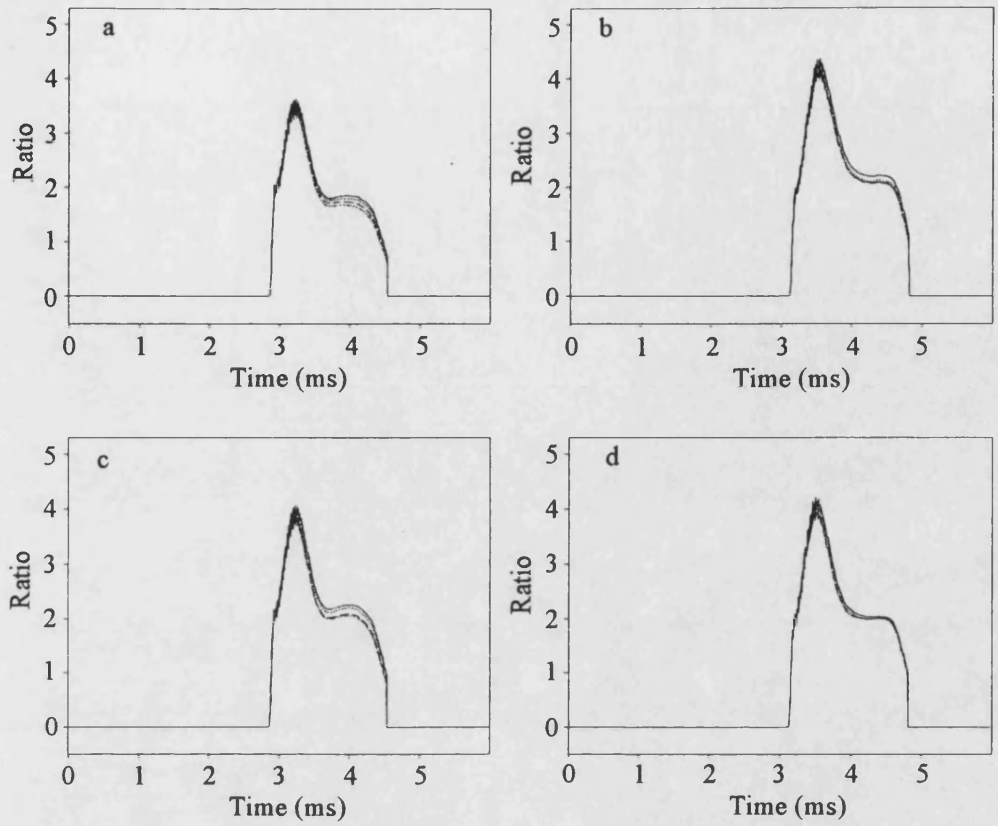


Fig. 6.48 - High resistance fault discrimination ratios

6.9 Network Effects

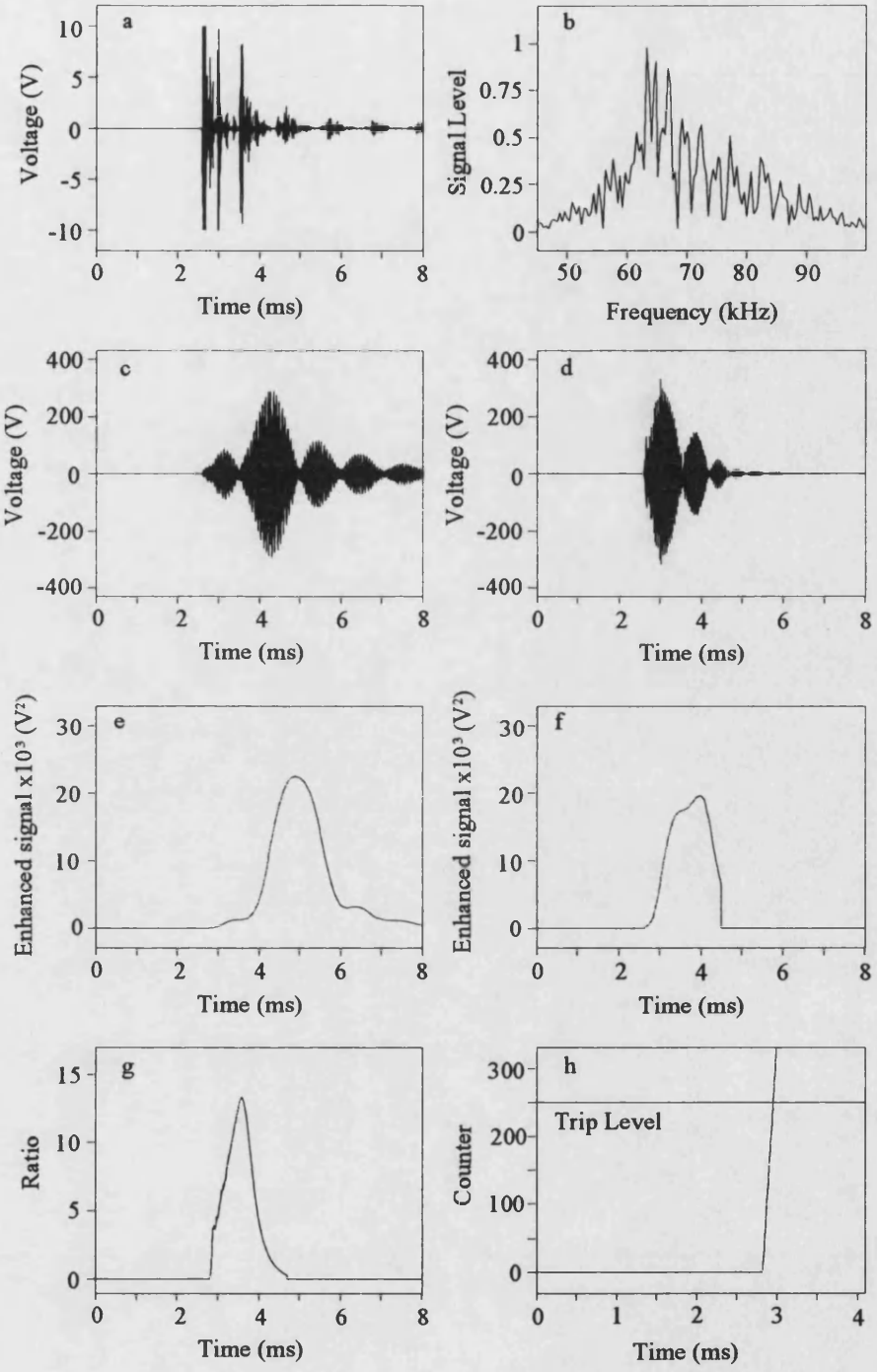
6.9.1 Variation in Source Capacities

This technique is not significantly affected by the source capacities at the ends of the circuit being protected. This can be seen by changing the source capacities of the symmetrical tee circuit of Fig. 6.1a to 35 GVA and 5 GVA at ends P and Q respectively and then applying a 45° phase a to earth fault at F_3. Comparing the end

P and Q mode V_x waveforms (Figs. 6.49, 6.50) to the corresponding results with source capacities of 20 GVA at each end (Figs. 6.16, 6.17) it can be seen that there is very little visible difference between them. This is because the line trap and busbar shunt capacitance forms a strong barrier to the tuned band of frequencies at each end of the circuit making the technique insensitive to changes in the source side networks.

6.9.2 Line Loading Effects

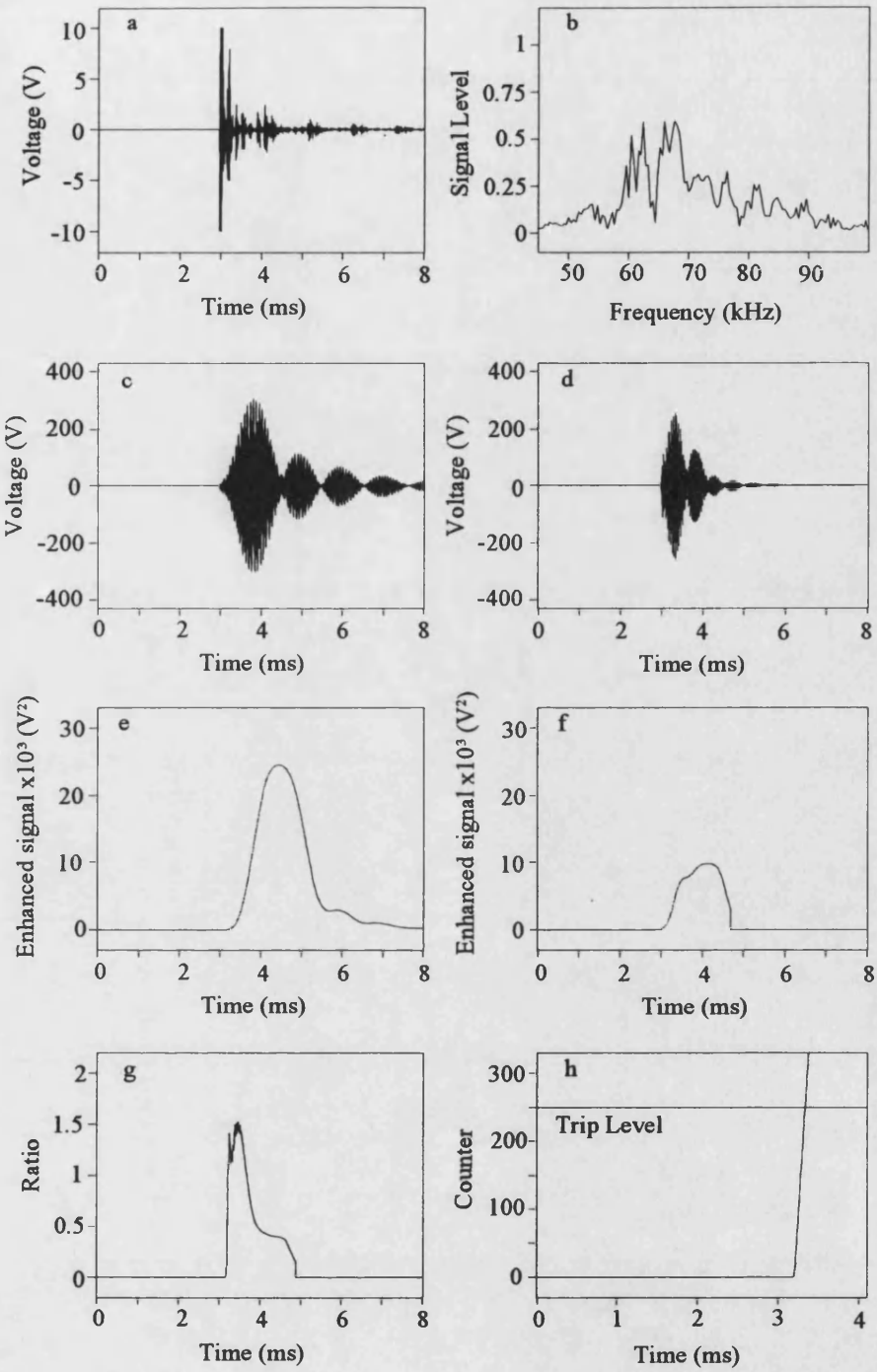
Figures 6.51 and 6.52 show the effect of prefault loading of the transmission lines when an a phase to earth fault is applied at 45° on the circuit of Fig. 6.1a at F_3. The phase angles of the source voltages at end P are reduced by 10° relative to the sources at ends Q and R. There are only very minor differences between these responses and the no load case (Figs. 6.16, 6.17). The amount of HF signals generated by the fault are not affected by the amount of line loading and so the scheme's performance is not altered.



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

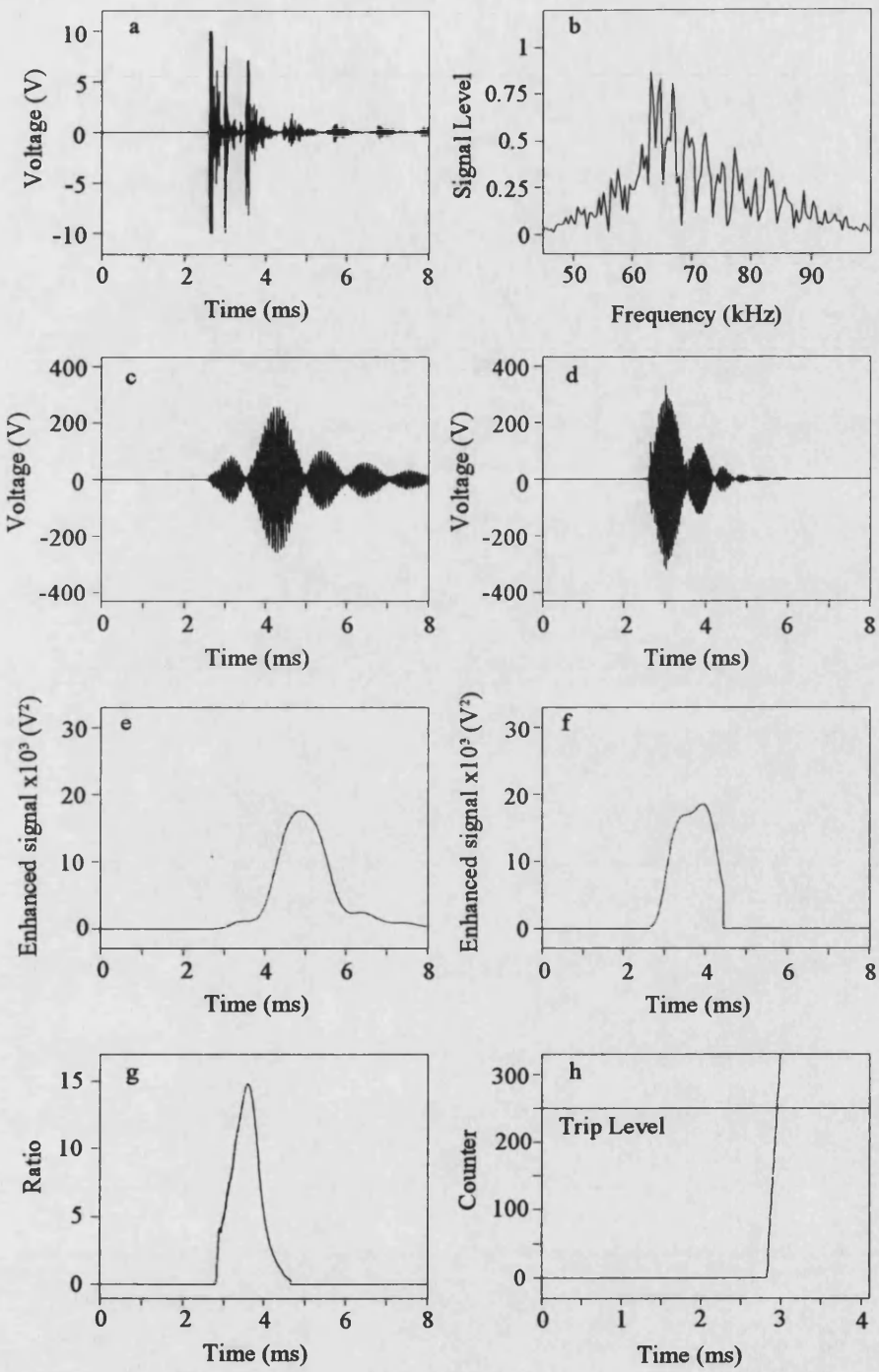
Fig. 6.49 - Effect of source capacity variation at end P



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

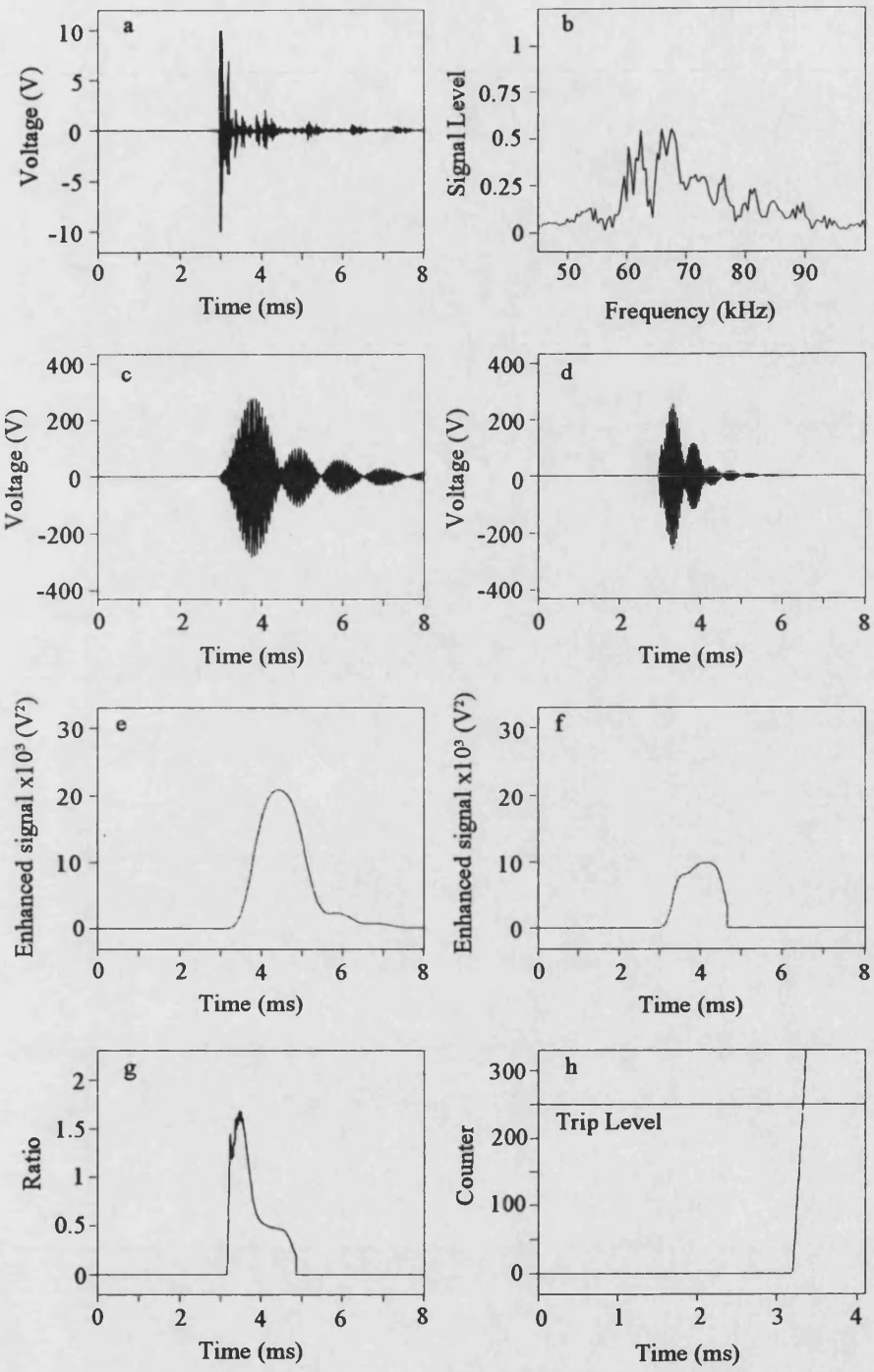
Fig. 6.50 - Effect of source capacity variation at end Q



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.51 - Effect of line loading at end P



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.52 - Effect of line loading at end Q

6.9.3 Effect of Circuit Configuration

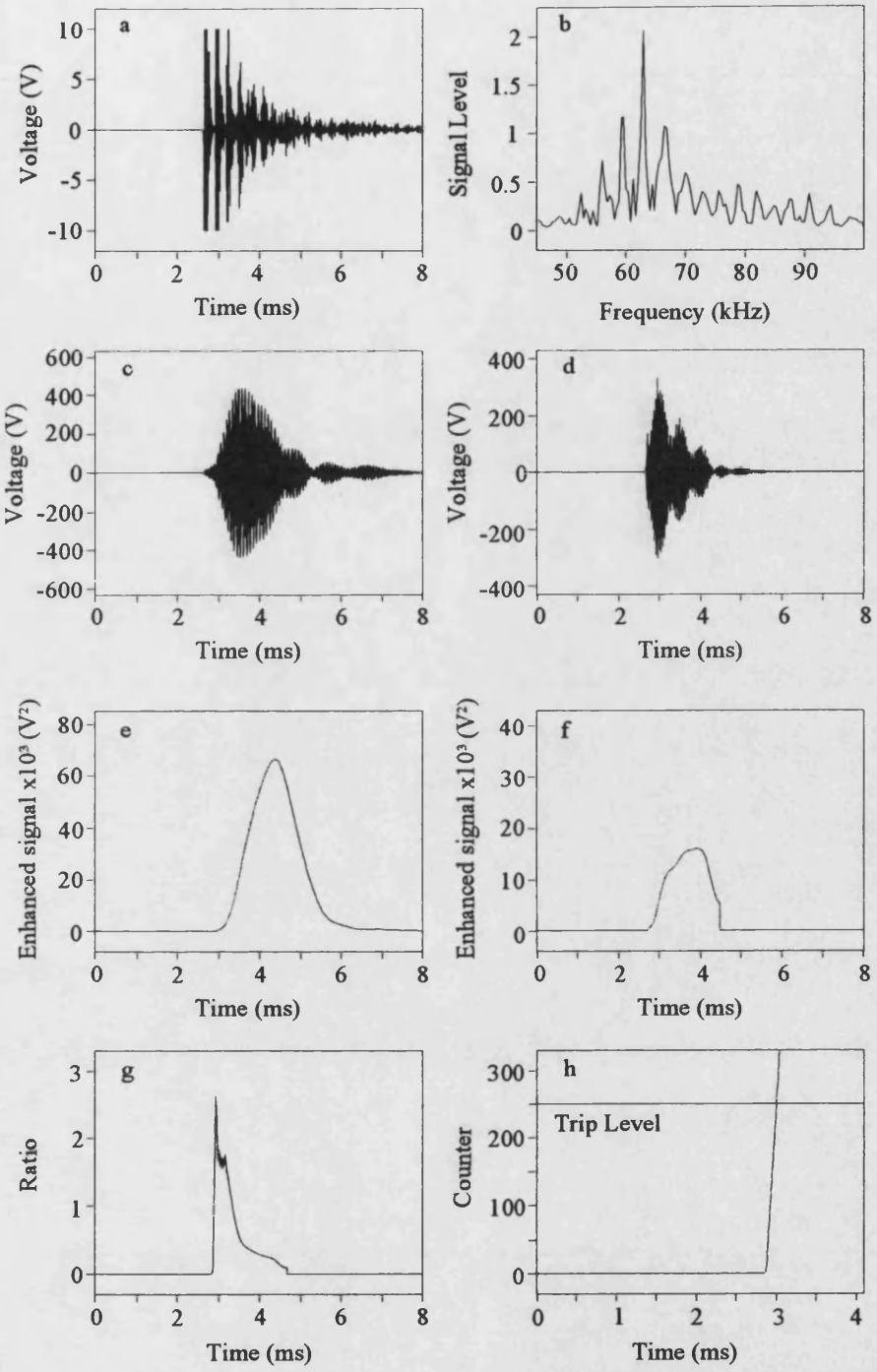
The performance of the scheme for different circuit configurations is best demonstrated by applying a variety of faults to the symmetrical and unsymmetrical tee networks of Fig. 6.1. The faults cover a wide selection of fault positions, inception angles and types, and combine a number of effects that have been discussed. The results are summarised in Table 6.6.

Table 6.6 - Effect of circuit configuration on trip times

N/O - No Operation

Fault characteristics Note: Fault angle is the angle of V_a at end P			Time to trip after fault inception (ms)					
			End P		End Q		End R	
Position	Angle	Type	Mode V_x	Mode V_y	Mode V_x	Mode V_y	Mode V_x	Mode V_y
F_4	-120°	ABC	0.435	0.435	0.845	0.840	0.845	0.840
F_5	45°	AB	0.515	0.505	0.785	0.770	0.785	0.770
F_9	-30°	AB-E	0.505	0.535	0.530	0.545	0.880	0.855
F_{10}	105°	C-E	0.645	0.650	0.390	0.395	0.710	0.710
F_{11}	-155°	ABC-E	0.815	1.290	0.730	0.755	0.355	1.130
F_{12}	95°	B-E	N/O	N/O	N/O	N/O	N/O	N/O
F_{13}	-135°	BC	N/O	N/O	N/O	N/O	N/O	N/O

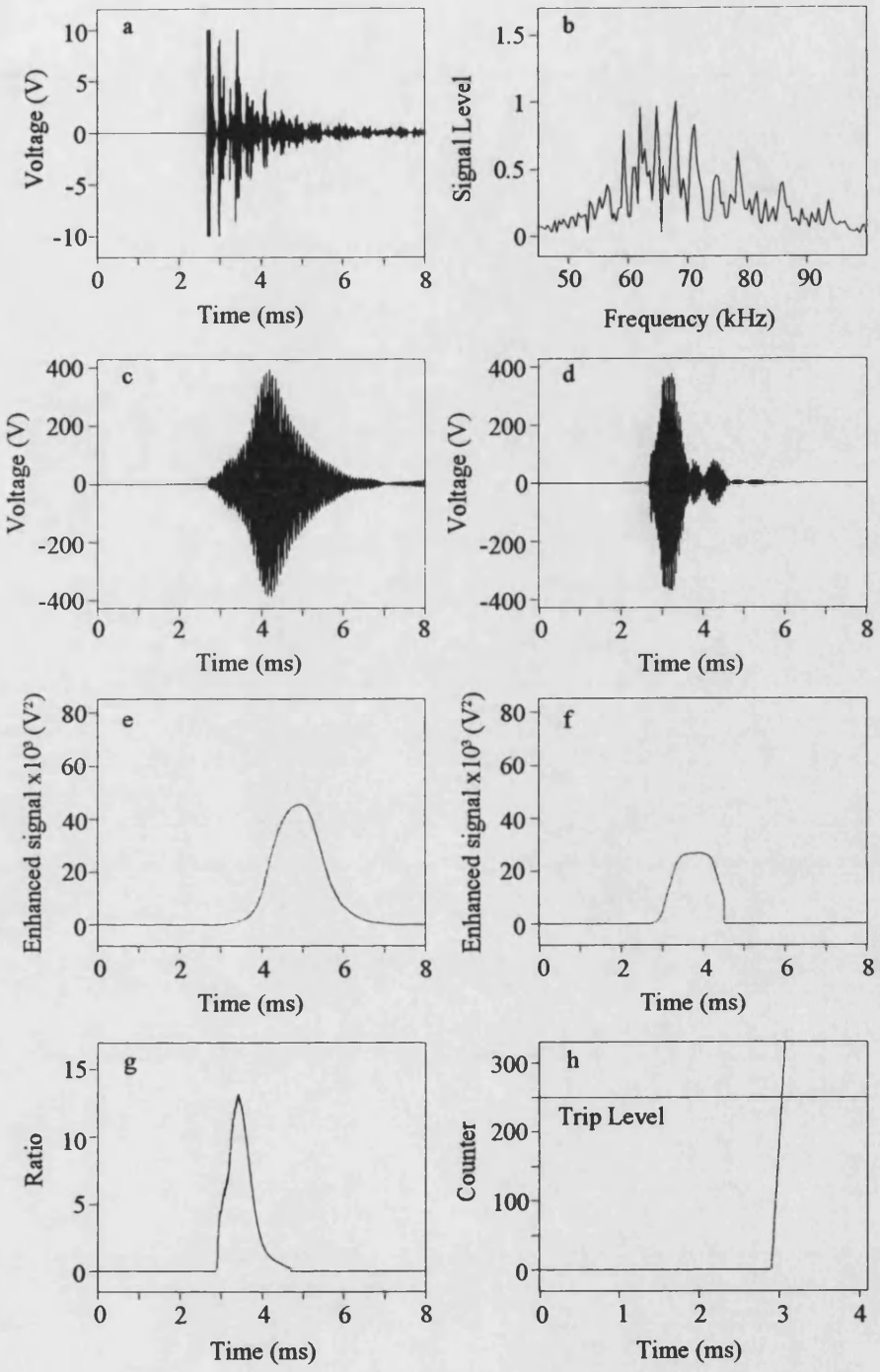
Figures 6.53-6.55 show the mode V_x outputs at the three ends for the fault at F_9 on the unsymmetrical tee network of Fig. 6.1b. This is a phase to phase fault and so large amounts of HF signals are generated. Consequently, the signals captured by the stack tuners have to be clipped. The magnitudes of the signals received at each end is determined by the distance between the fault and the measurement equipment. The end R signals are attenuated the most, as they travel the furthest distance. However, this means that they are clipped less and so there is lower distortion to the signals entering the protection relay. This can be clearly seen by comparing the frequency spectra and the filter outputs at the three line ends (Figs. 6.53b,c,d, 6.54b,c,d, 6.55b,c,d). The discrimination ratios at the terminals all exceed one, less than a millisecond after fault inception, with the time of the trip decisions being strongly influenced by the travel time of the signals from the fault to the line ends.



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

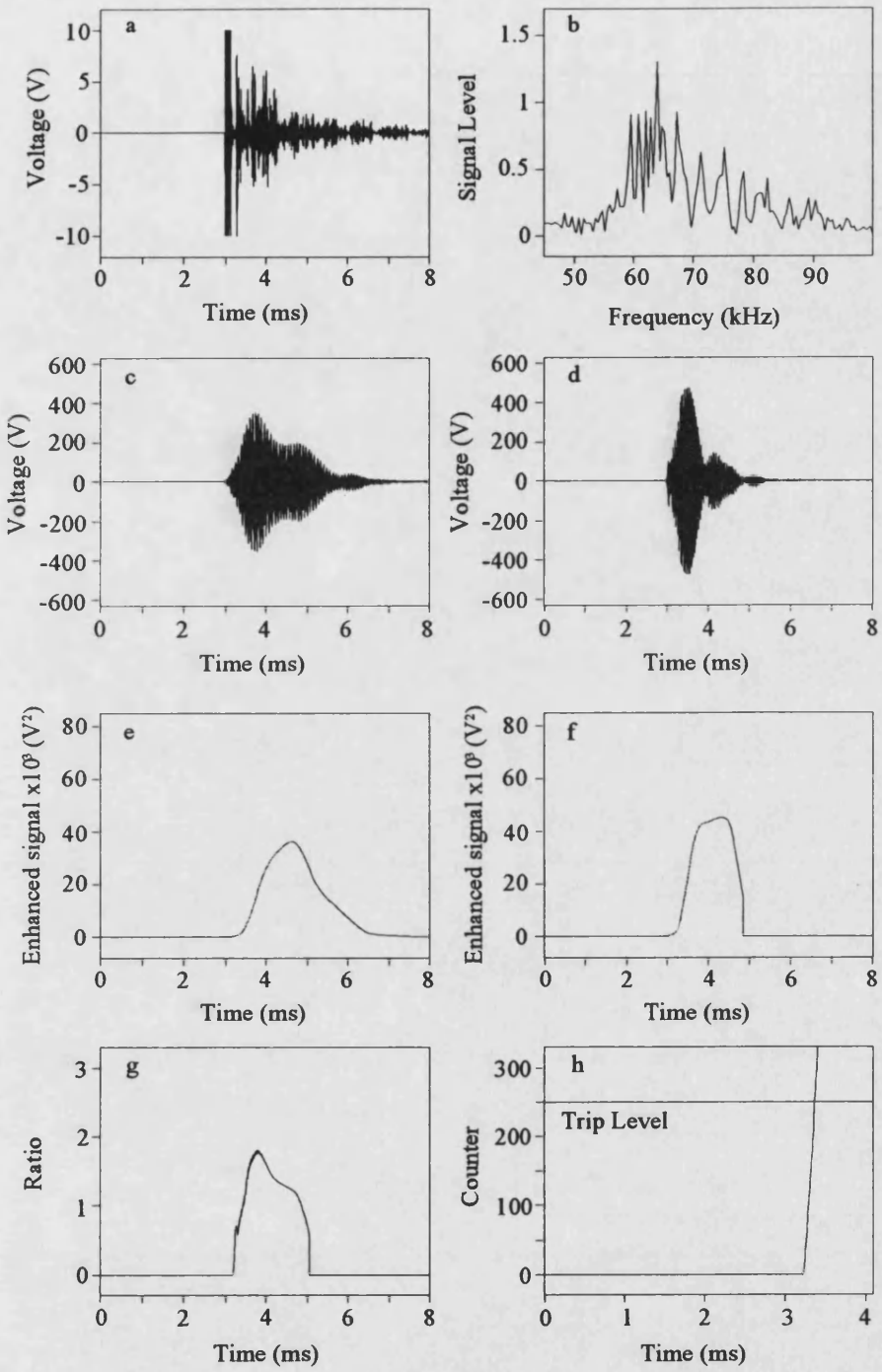
Fig. 6.53 - A-B-E fault at F_9 end P response



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.54 - A-B-E fault at F_9 end Q response



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

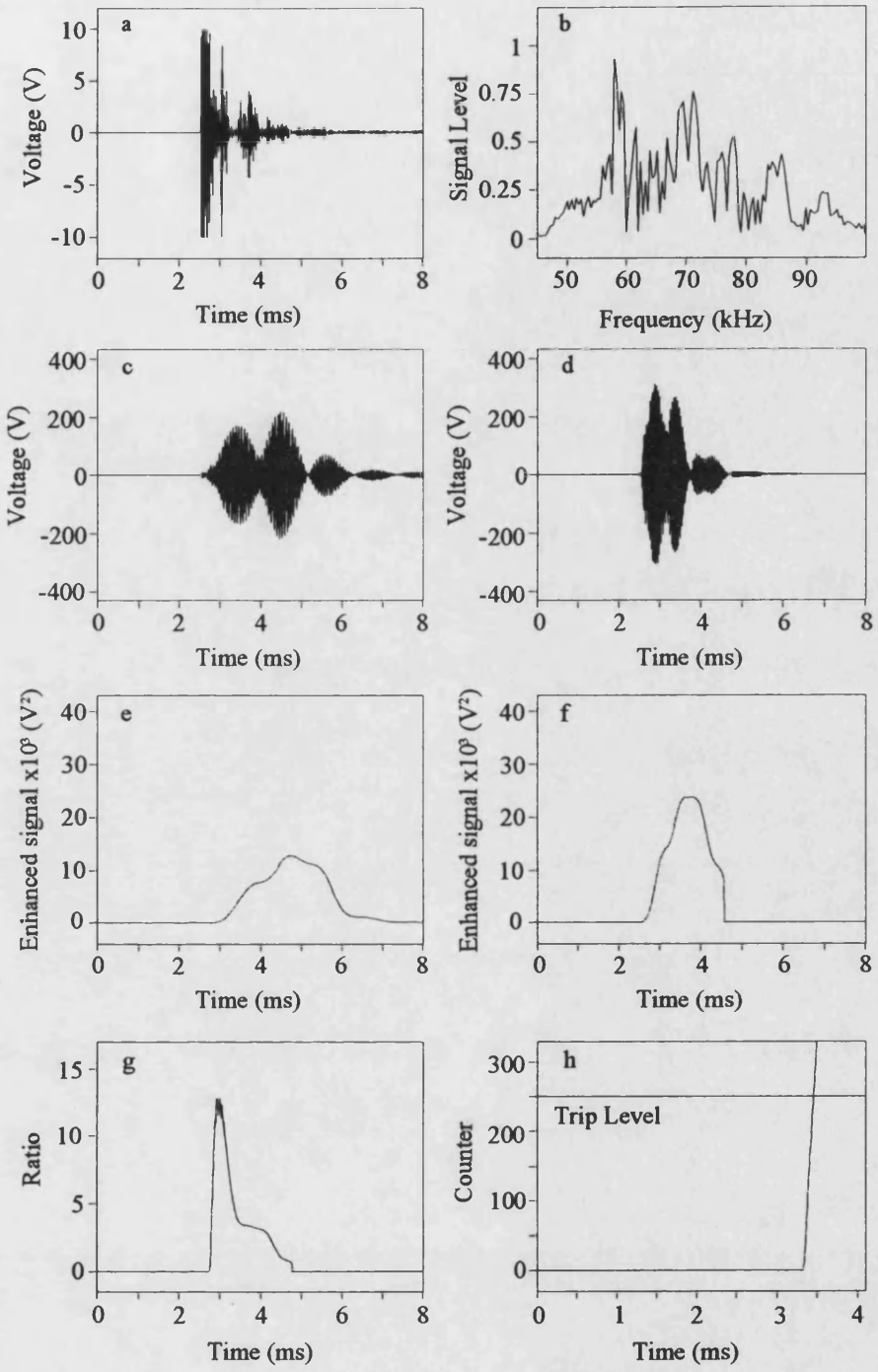
Fig. 6.55 - A-B-E fault at F_9 end R response

6.9.3.1 Feed Around Path Performance

Feed around paths can cause problems for some protection techniques, as discussed in section 2.4.1.1. This method however, is not affected by this situation. A single phase to earth fault is applied to phase c, 10 km from end P (F_8 in Fig. 6.1b) at an inception angle of 60° relative to the phase c voltage. The source and network configuration and the position of the fault cause current to flow from end Q, out through end R, along the feed around path and then through end P to the fault point, in addition to the fault current which flows directly from end Q to the fault point.

The mode V_y waveforms at each end can be seen in Figs. 6.56, 6.57 and 6.58. These show that the feed around path does not affect the nature of the signals that are recorded. The main influencing factors are the fault inception angle and the distance travelled from the fault. Examining the faulted phase currents at the ends (Fig. 6.59a), shows that as expected, the current at end R is almost 180° out of phase with the currents at the other ends. Its magnitude is much lower as end R is a very weak source whereas end P is a slightly stronger source which has the extra contribution from the feed around path.

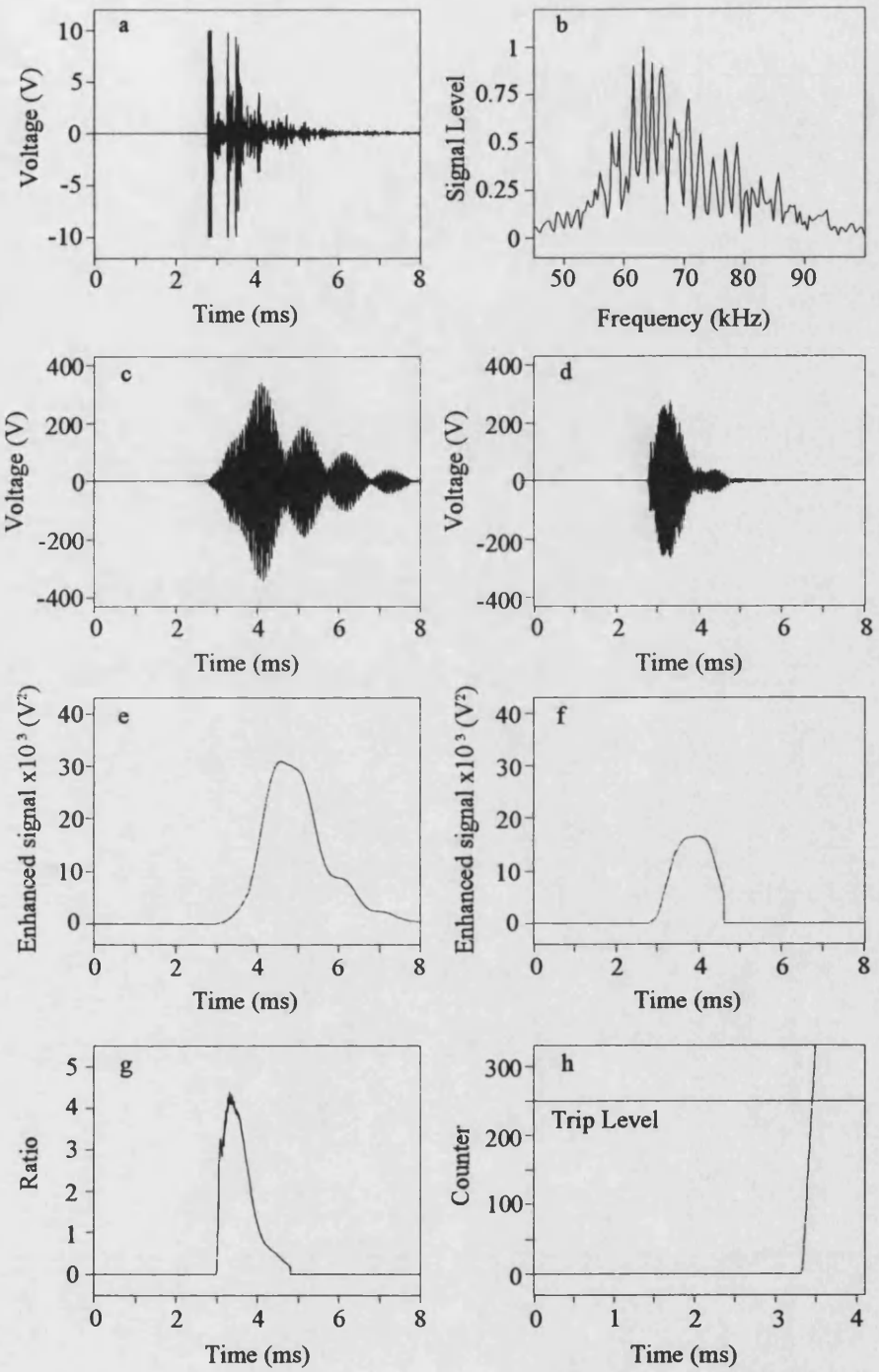
Inspite of the reversal of the current flow at end R, the discrimination ratios at all three ends are all well above one. A comparison of the mode V_y signals is shown in Fig. 6.59b. Both of the modes trip counter outputs exceed the threshold level at all three ends a short time after fault inception (Fig. 6.59c,d), the actual times are shown in Table 6.7.



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

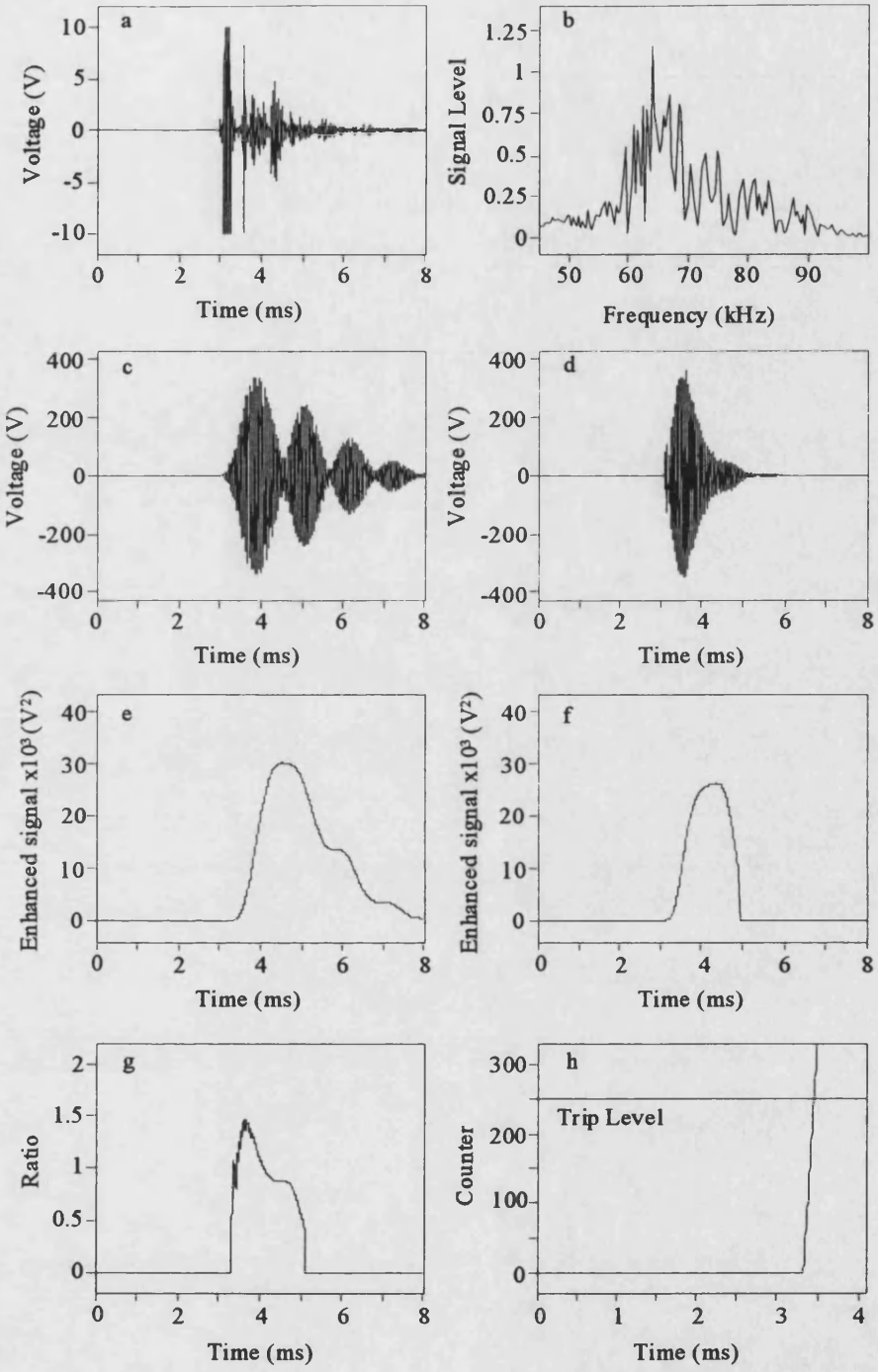
Fig. 6.56 - Feed around path performance at end P



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

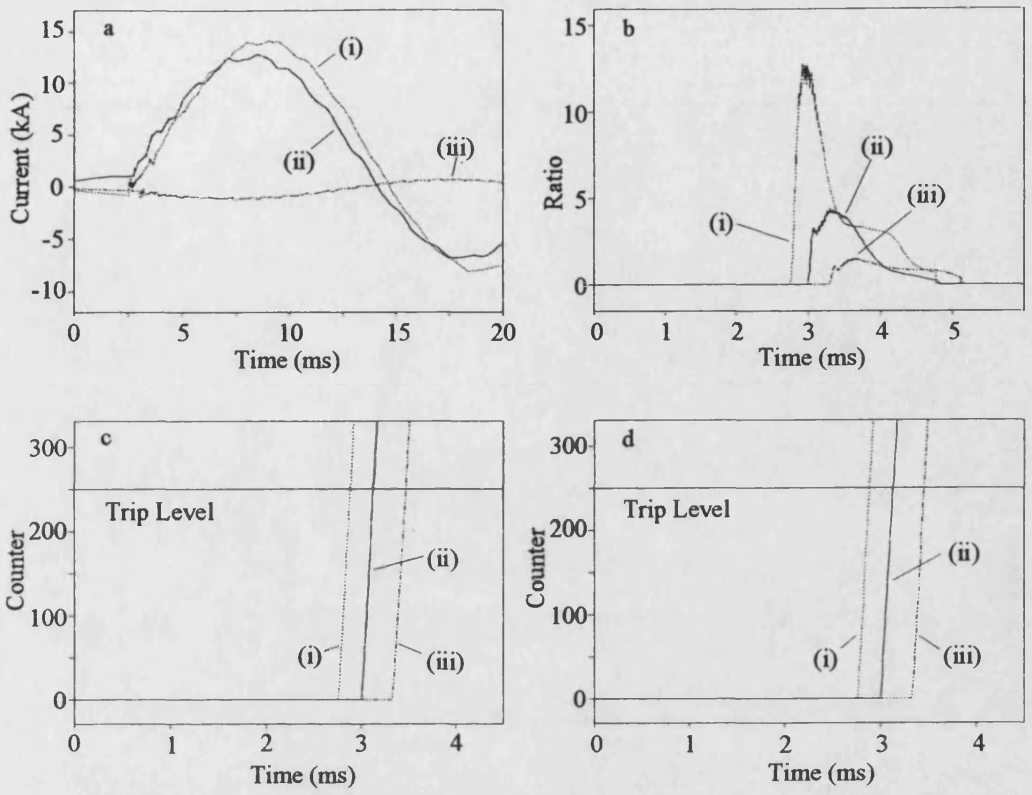
Fig. 6.57 - Feed around path performance at end Q



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 6.58 - Feed around path performance at end R



a Faulted phase currents
b Mode V_y discrimination ratios
c Mode V_x counter outputs
d Mode V_y counter outputs
Fault inception, $t_f = 2.5$ ms
(i) End P
(ii) End Q
(iii) End R

Fig. 6.59 - Feed around path performance at ends P, Q, R

Table 6.7 - Feed around path trip times

Mode	Trip time after fault inception (ms)		
	End P	End Q	End R
V_x	0.390	0.635	0.970
V_y	0.390	0.635	0.955

6.9.3.2 Alternative Operating Conditions

There may be occasions when the teed circuit is not being used under its normal operating conditions. One or two of the line terminals may be disconnected because of maintenance, for example. Other protection schemes, such as Current Differential protection, may have to have the settings changed to cope with this scenario. They may not even be able to protect the circuit satisfactorily if it is only being supplied from one terminal.

This does not cause any problems for this technique as each end only relies on information that is gathered locally. The nature of the captured HF signals are not affected by the status of the line ends and so the technique behaves correctly. The results for three examples are shown in Table 6.8. In these cases the relevant terminals are opened between the source impedances and the line traps, so the relays are able to give trip outputs at the open ends. In practice these signals would have to be suppressed so that a trip signal is not sent to an already open circuit breaker. This could be done by simply turning off the necessary relay as no information is exchanged between any of the relays.

Table 6.8 - Alternative operation performance

Fault characteristics Note: Fault angle is the angle of V_a at end P				Time to trip after fault inception (ms)					
				End P		End Q		End R	
Pos^n	Angle	Type	Open ends	Mode V_x	Mode V_y	Mode V_x	Mode V_y	Mode V_x	Mode V_y
F_9	-145°	ABC	P	0.630	0.515	0.530	0.530	0.885	0.875
F_8	15°	BC-E	P, R	0.560	1.600	0.615	0.685	1.215	1.350
F_{11}	5°	A-E	R	0.985	0.985	0.745	0.745	0.385	0.370

If the line were disconnected just in front of the coupling capacitor , the scheme would still perform correctly. The relays at the open ends would not detect the internal fault but this would not matter because the circuit breakers would be open already.

6.9.3.3 Double Circuit Performance

The performance of the technique was also evaluated for a double circuit teed network. The transmission line was modelled as a six phase line to take into account the mutual coupling between the phase conductors. The conductor and phase arrangements are shown in Fig. 6.60.

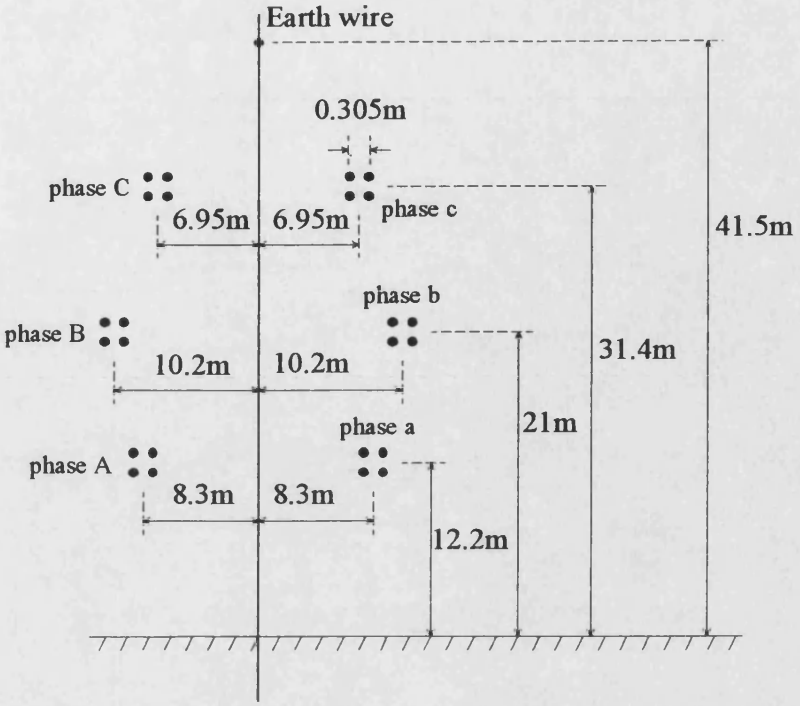


Fig. 6.60 - Double circuit line configuration

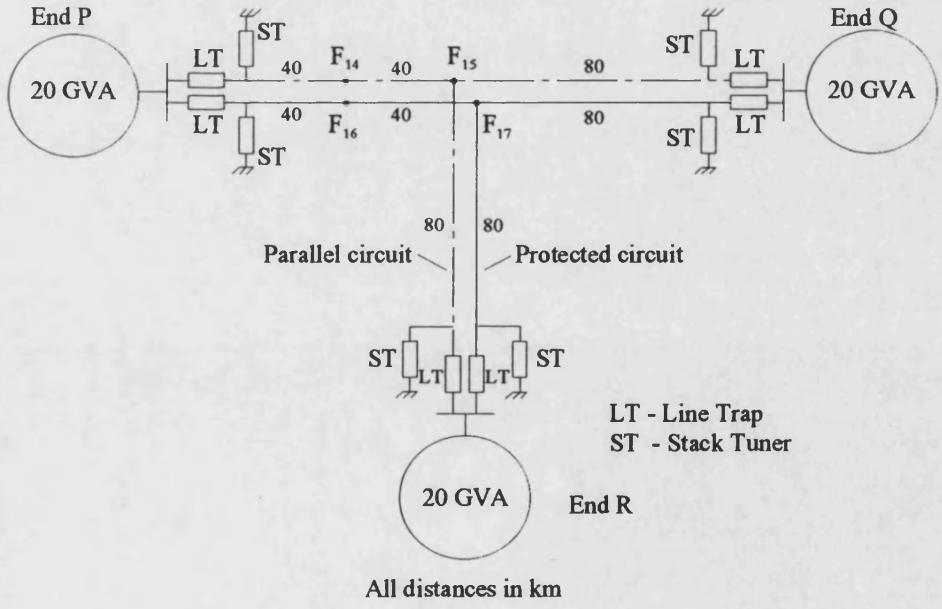


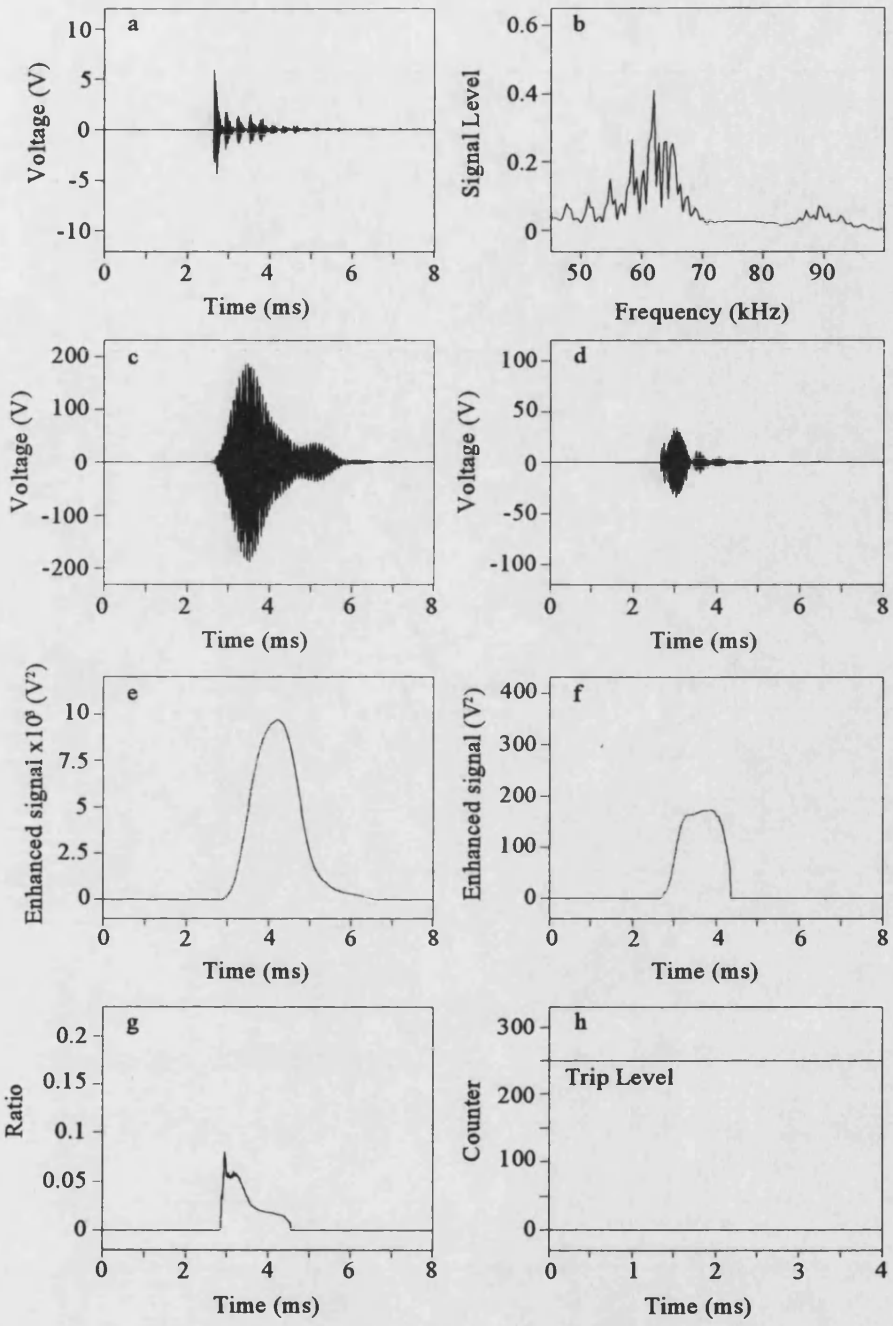
Fig. 6.61 - Double circuit teed network

A symmetrical tee network was used and the fault positions are shown in Fig. 6.61. The lines were assumed to be fully transposed which equalises the mutual coupling between the individual conductors.

Table 6.9 summarises the scheme's performance for a selection of faults on the adjacent parallel line and the protected line. The external faults on the adjacent line do not cause a trip decision to be made and the internal faults are both recognised in less than a millisecond after fault inception. The waveforms for the faults at F_{14} and F_{16} are shown in Figs. 6.62-6.65 and there are no major differences between the single and the double circuit cases. The end R results are not shown as they are identical to the end Q responses because of the symmetry of the circuit being studied.

Table 6.9 - Double circuit teed network performance

Fault characteristics Note: Fault angle is the angle of V_a at end P			Time to trip after fault inception (ms)			
			End P		End Q	
Pos^n	Angle	Type	Mode V_x	Mode V_y	Mode V_x	Mode V_y
F_{14}	-75°	C-E	N/O	N/O	N/O	N/O
F_{15}	-90°	AB-E	N/O	N/O	N/O	N/O
F_{16}	-75°	C-E	0.505	0.505	0.780	0.780
F_{17}	-90°	AB-E	0.650	0.650	0.650	0.650



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig.6.62 - External fault mode V_x response at end P for double circuit network

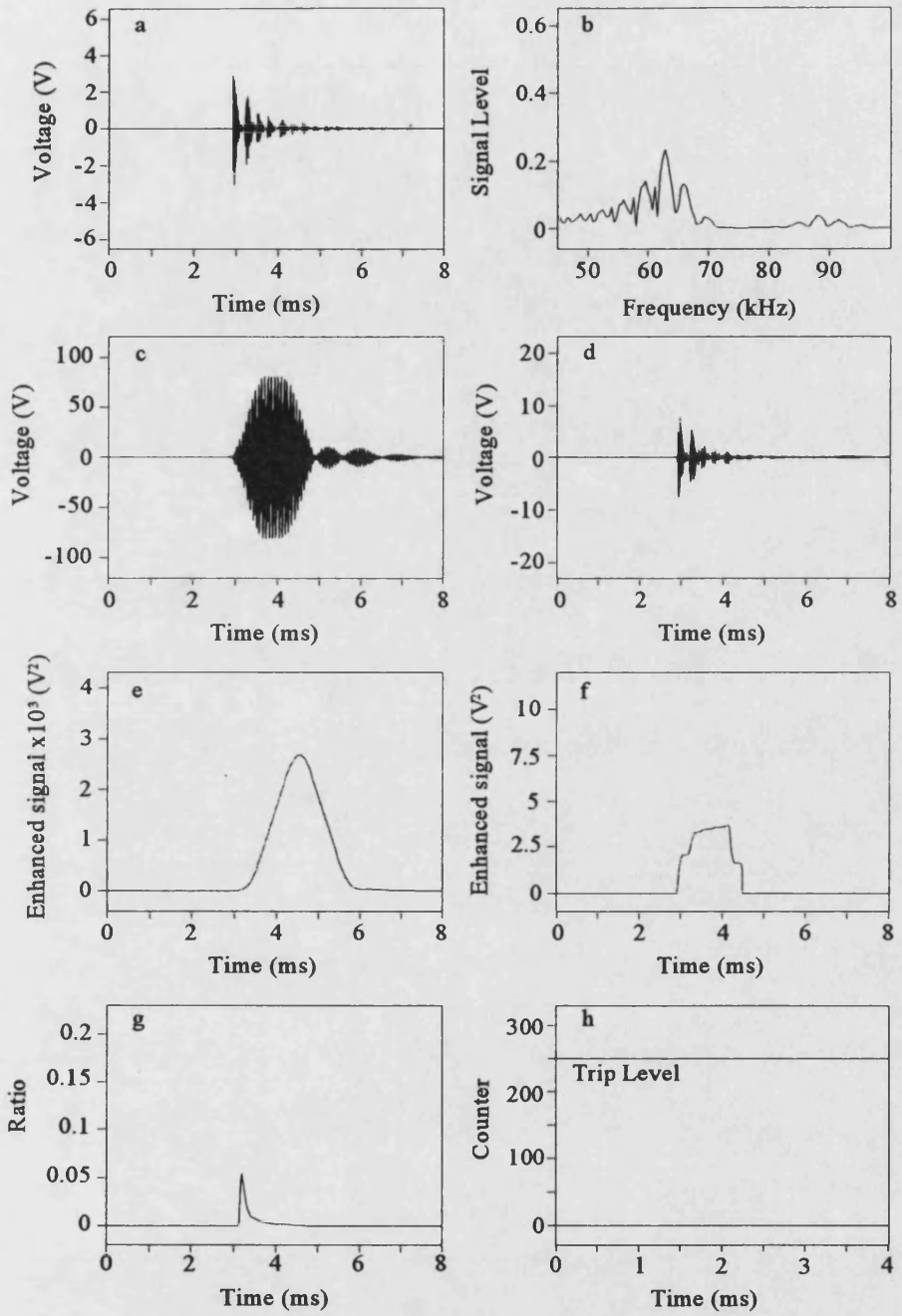
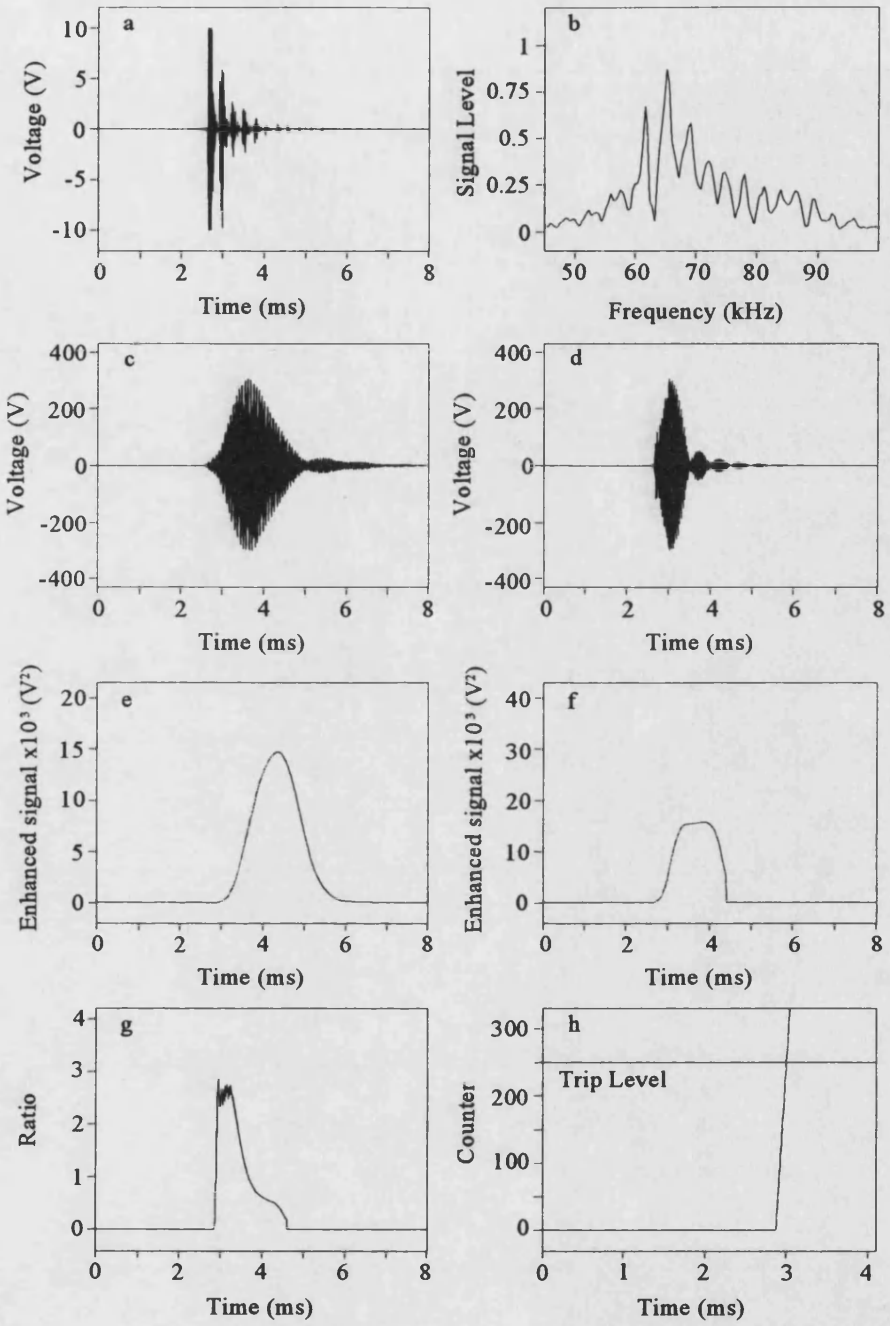


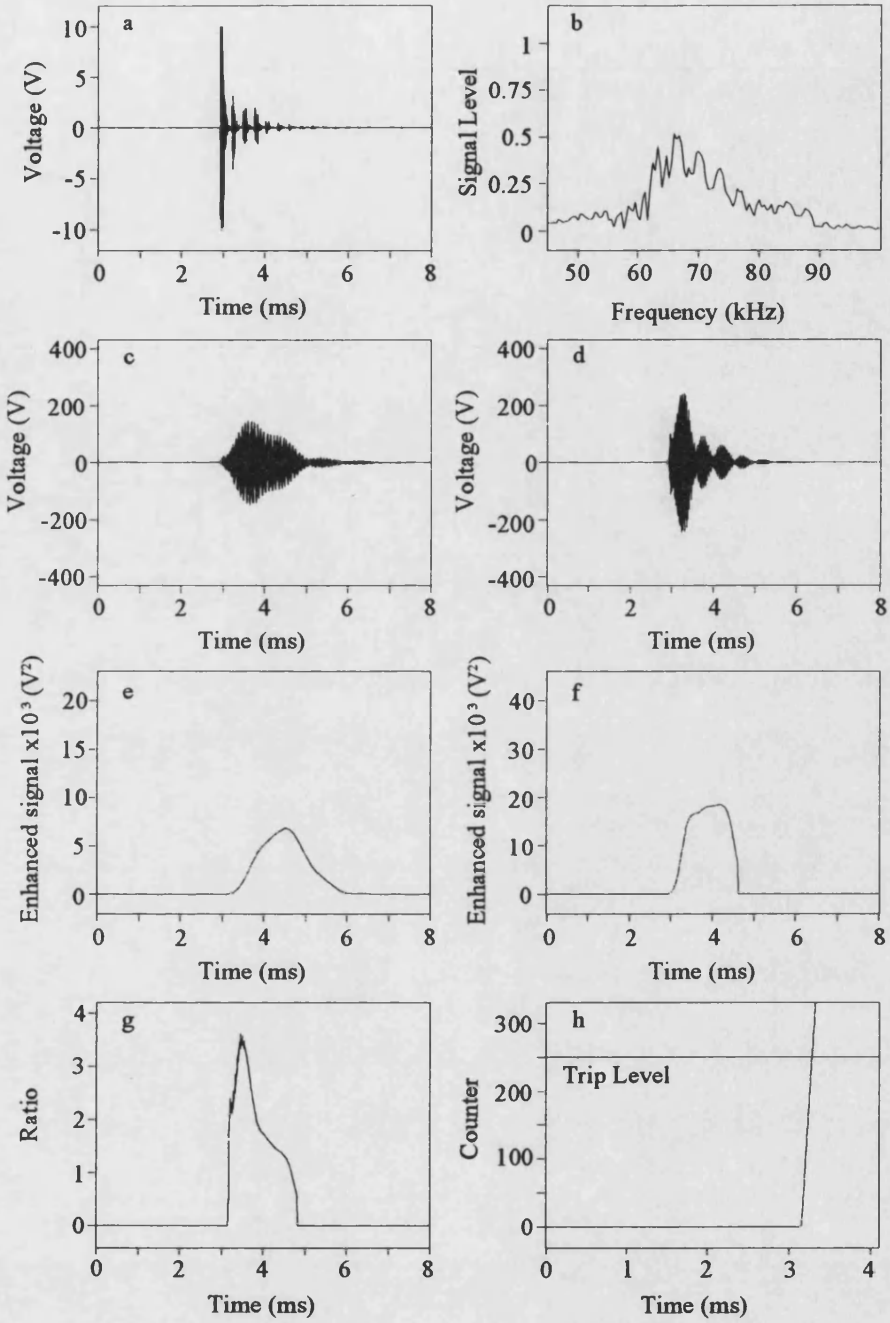
Fig.6.63 - External fault mode V_x response at end Q for double circuit network



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, t_f = 2.5 ms

Fig.6.64 - Internal fault mode V_x response at end P for double circuit network



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig.6.65 - Internal fault mode V_x response at end Q for double circuit network

6.9.4 Parameter Sensitivity

The parameter values of the components in the line trap and stack tuner can vary over time. This may be due to environmental effects or component aging. This deviation from their nominal values can de-tune the devices by shifting their centre frequencies or by affecting their bandwidths. These non-algorithmic errors can have a detrimental effect on relay performance and so a sensitivity analysis was carried out to assess the consequences of these variations.

Table 6.10 summarises the relay performance obtained for variations of $\pm 5\%$ in both the line trap and stack tuner parameters. This indicates that there is little effect on the performance of the relay for both internal and external faults. The relay can cope with these small errors in the analogue signal measurements because of the robustness of the digital filter design and the decision logic that is incorporated within the relay algorithm.

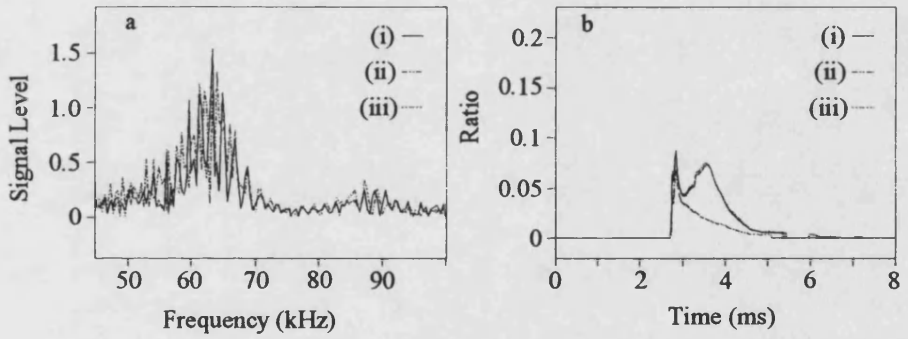
Table 6.10 - Parameter sensitivity at end P (symmetrical tee)

Parameters as shown in Fig. 3.1

N/O - No Operation

Fault Type	Parameter Varied	Variation	End P Operating Time (ms)		Correct Operation
			Mode V_x	Mode V_y	
Internal 45° a-earth fault at F_1	None	-	0.42	0.35	Yes
	C_p	+5%	0.42	0.35	Yes
		-5%	0.42	0.35	Yes
	L_p	+5%	0.42	0.35	Yes
		-5%	0.45	0.35	Yes
	C_1	+5%	0.42	0.35	Yes
		-5%	0.42	0.35	Yes
	L_2	+5%	0.425	0.355	Yes
		-5%	0.415	0.35	Yes
External 45° a-earth fault at F_2	C_p	+5%	N/O	N/O	Yes
		-5%	N/O	N/O	Yes
	L_p	+5%	N/O	N/O	Yes
		-5%	N/O	N/O	Yes
	C_1	+5%	N/O	N/O	Yes
		-5%	N/O	N/O	Yes
	L_2	+5%	N/O	N/O	Yes
		-5%	N/O	N/O	Yes

The stray capacitance of the busbars at the line ends was set to a value of 0.1 μF, which is typical for a 400 kV network. The sensitivity of the scheme to changes in this value were also examined by altering C_s at all three ends to 0.01 μF and then to 0.2 μF for the same external fault. Figure 6.66 shows that there is very little difference in the frequency spectra of the stack tuner outputs or the discrimination ratios at end P.



a Frequency spectra at end P b Discrimination ratios at end P (i) $C_s = 0.1\mu F$

Fault inception, $t_f = 2.5$ ms (ii) $C_s = 0.01\mu F$

(iii) $C_s = 0.2\mu F$

Fig. 6.66 - Effect on the algorithm of varying busbar capacitance

CHAPTER 7

COMPOSITE CIRCUIT PERFORMANCE

7.1 Underground Cable Modelling

Single phase coaxial cables are generally used for EHV applications as they are the only practical way of carrying the necessary load current and maintaining the insulation requirements. The underground cables modelled in this thesis were based on 400 kV oil filled cables used by NGC. A cross section of a cable and the relative buried positions of the cable circuit are shown in Fig. 7.1.

A copper conductor is used with a nominal cross sectional area of 2000 mm^2 which has an oil duct running through its centre. The oil is kept under pressure and is used to remove some of the heat of the conductor, as it carries load current. This is covered by an insulating layer of oil impregnated paper. Surrounding this is a conducting lead alloy sheath. The cable is protected by a 1% tin bronze tape armour which is covered by a high density polyethylene (HDPE) outer coating. The sheath is separated from the armour by an insulating bedding material. The parameters of the cable materials are shown in Table 7.1. The earth resistivity was taken to be 100 Ωm.

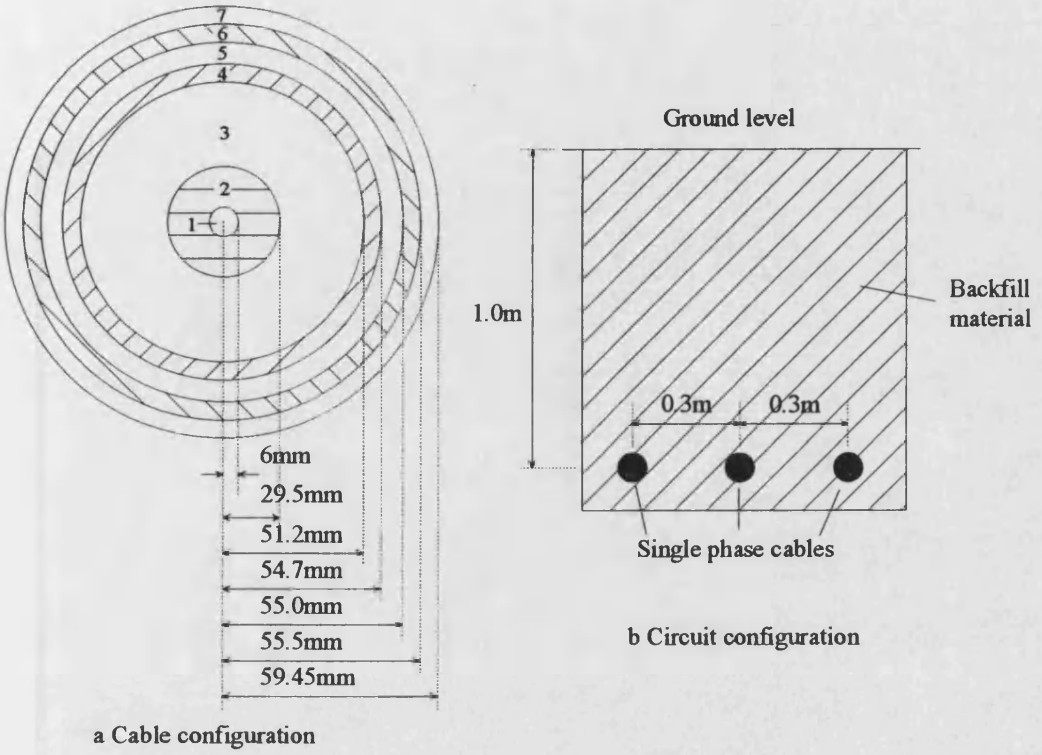


Fig. 7.1 - Underground cable configuration

The cables are buried in a horizontal configuration 1 m below the surface (Fig. 7.1b). Water pipes are frequently buried alongside the power conductors to reduce the temperature of the soil as it is heated by the cables. These were not modelled as the heating effects of the cable and the surrounding area were not taken into account.

Table 7.1 - Cable material parameters

Material	Conductivity, ρ x 10^{-8}(Ωm)	Relative Permeability, μ_r	Relative Permittivity, ε_r
1. Oil duct	-	-	-
2. Copper conductor	1.724	1.0	-
3. Insulating paper	-	1.0	3.8
4. Lead alloy sheath	21.264	1.0	-
5. Bedding material	-	1.0	3.5
6. Tin bronze armour	1.70	1.0	-
7. HDPE covering	-	1.0	2.8

The cables were modelled using the cable constants routine of the EMTP and the parameter frequency dependence is modelled using the J. R. Marti fitting algorithm [sim7]. The cables are split into 1 km major sections, each of which consist of three minor sections. At the end of each minor section, the sheath of phase a is

connected to the sheath of phase b, the sheath of phase b is connected to the sheath of phase c, and the sheath of phase c is connected to the sheath of phase a (Fig. 7.2). This *crossbonding* of the cable sheaths reduces the losses due to sheath currents while decreasing the overvoltages that would occur if the cable sheath were grounded at regular intervals or ungrounded. The sheaths are then solidly grounded at each end of the length of cable.

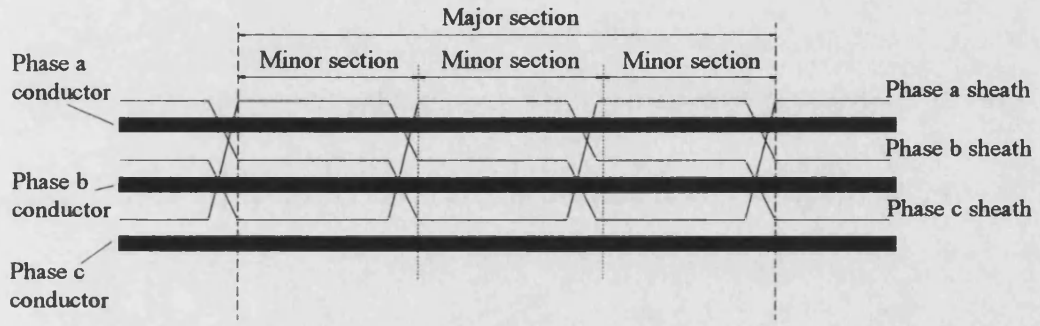


Fig. 7.2 - Underground cable crossbonding

Underground cables have a much higher attenuation rate than overhead lines and the modal propagation velocities are much slower. Tables 7.2 and 7.3 show a comparison of the line and cable modal parameters at 50 Hz. The propagation velocities of the three overhead line modes are all very close to the speed of light (300 km/ms). The underground cable modal velocities are significantly less than this. The three additional modes in the cable case are associated with the conducting nature of the cable sheaths. All of the cable modes attenuate signals much more than the line modes.

Table 7.2 - Line modal parameters

Mode	Propagation velocity (km/ms)	Modal attenuation (dB/km)
1	235.2	0.00059
2	294.7	0.00020
3	295.5	0.00021

Table 7.3 - Cable modal parameters

Mode	Propagation velocity (km/ms)	Modal attenuation (dB/km)
1	7.818	0.3396
2	7.634	0.2968
3	7.894	0.2776
4	98.98	0.0107
5	97.44	0.0087
6	108.3	0.0135

7.2 Protection System Differences

Many CAD studies were carried out to determine what revisions had to be made to the protection system so that it performed correctly on composite networks. The digital filter characteristics were varied along with the decision logic. Any information that was gained from this was then fed back to try to improve the teed circuit performance.

The basic protection system for the teed circuit case was found to be suitable for protecting the composite circuits with only a few adjustments. The cable characteristics slightly changed the frequency response of the whole circuit and so the restraint filter parameters were modified. The centre frequency of the restraint filter was lowered to 61 kHz and its bandwidth was increased to 2 kHz. The operate filter characteristics were not altered from the teed circuit system. The new filter coefficients are shown in Table 7.4 and the frequency response of both filters is shown in Fig. 7.3.

Table 7.4 - Restraint filter coefficients

G_0		0.0047653315	
a_0	1	b_0	1
a_1	0	b_1	0.66335499
a_2	-1	b_2	0.95734710
a_3	1	b_3	1
a_4	0.54150623	b_4	0.61055595
a_5	1	b_5	0.98310500
a_6	1	b_6	1
a_7	0.80735368	b_7	0.73232865
a_8	1	b_8	0.98349386

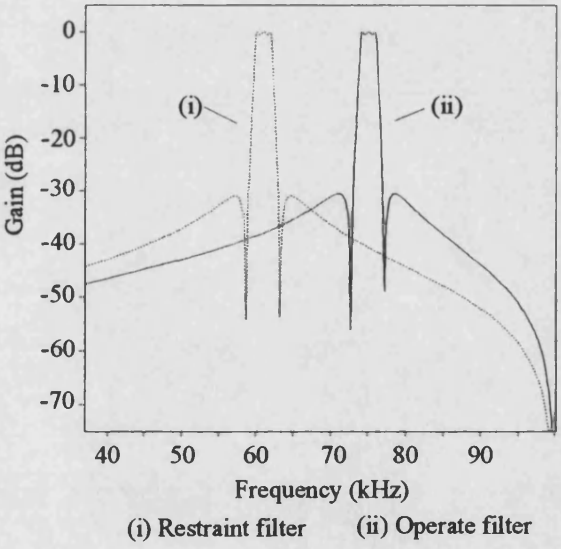
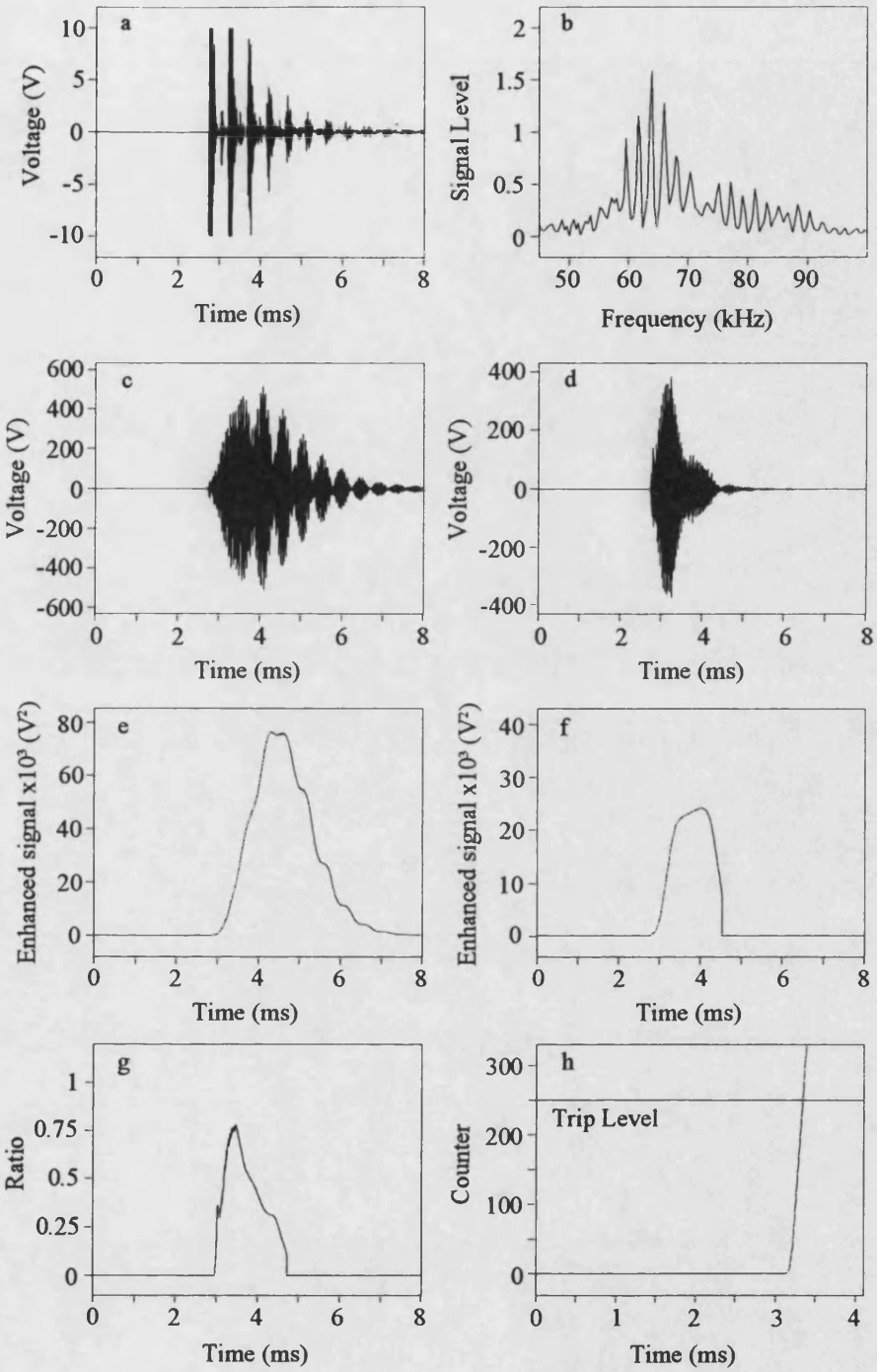


Fig. 7.3 - Filter frequency responses

The key features of the signals detected on the composite circuit were unchanged from the teed circuit case. Therefore, the original signal processing algorithm could successfully discriminate between internal and external faults. The counting algorithm is also the same as the teed circuit case (Table 7.5), but this is because it was actually fine tuned for the composite circuit case. After giving satisfactory results, it was tried with the teed circuit protection system. It improved the performance of the algorithm compared to the previous counting regime and so replaced the old regime.

Table 7.5 - Counting regime

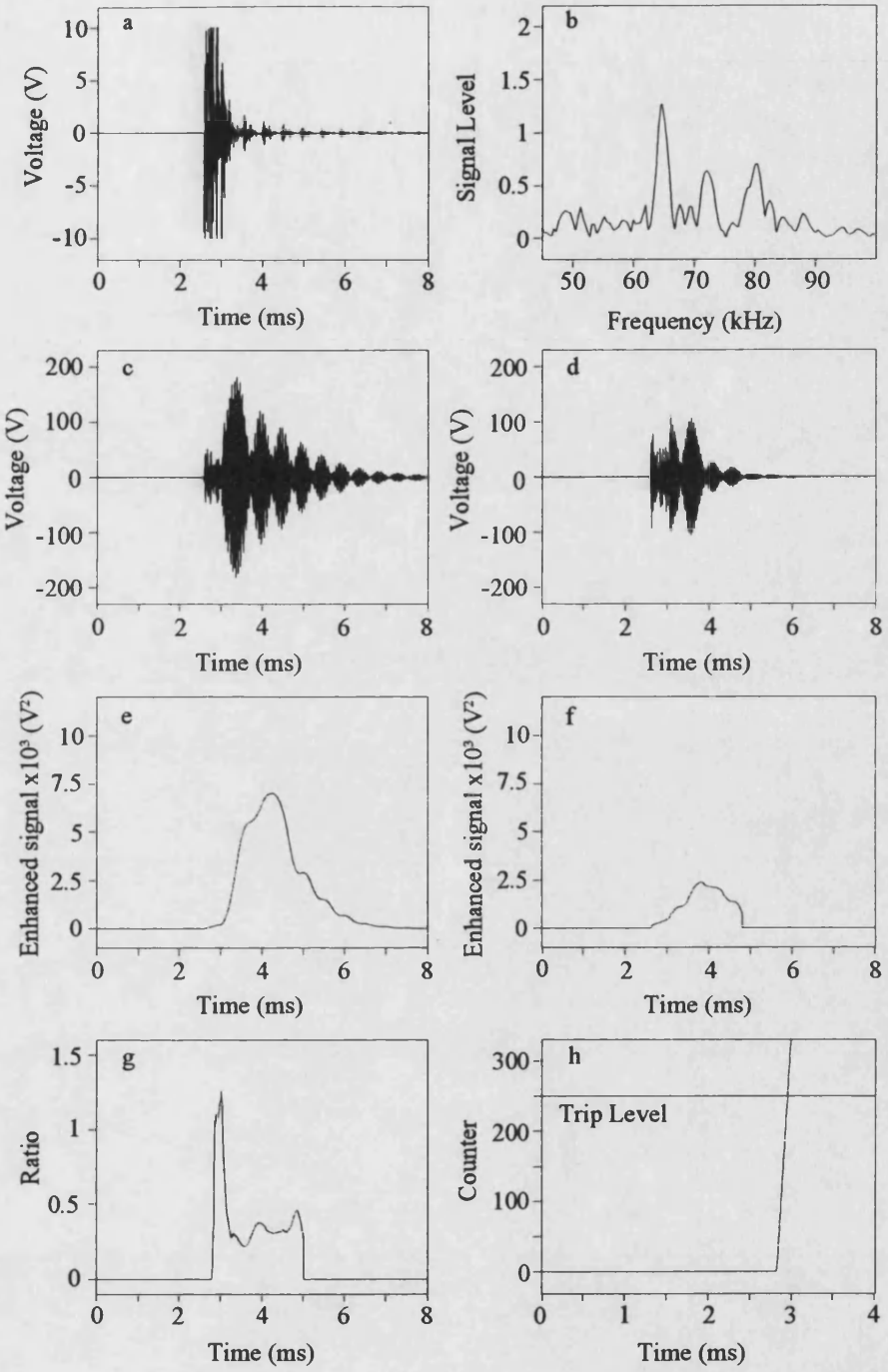
Discrimination Ratio, D_r	Counter Increment
$D_r \geq 0.8$	+ 10
$0.8 > D_r \geq 0.6$	+ 9
$0.6 > D_r \geq 0.5$	+ 4
$0.5 > D_r \geq 0.4$	+ 1
$0.4 > D_r \geq 0.1$	- 1
$0.1 > D_r \geq 0.005$	-3
$0.005 > D_r$	- 10



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

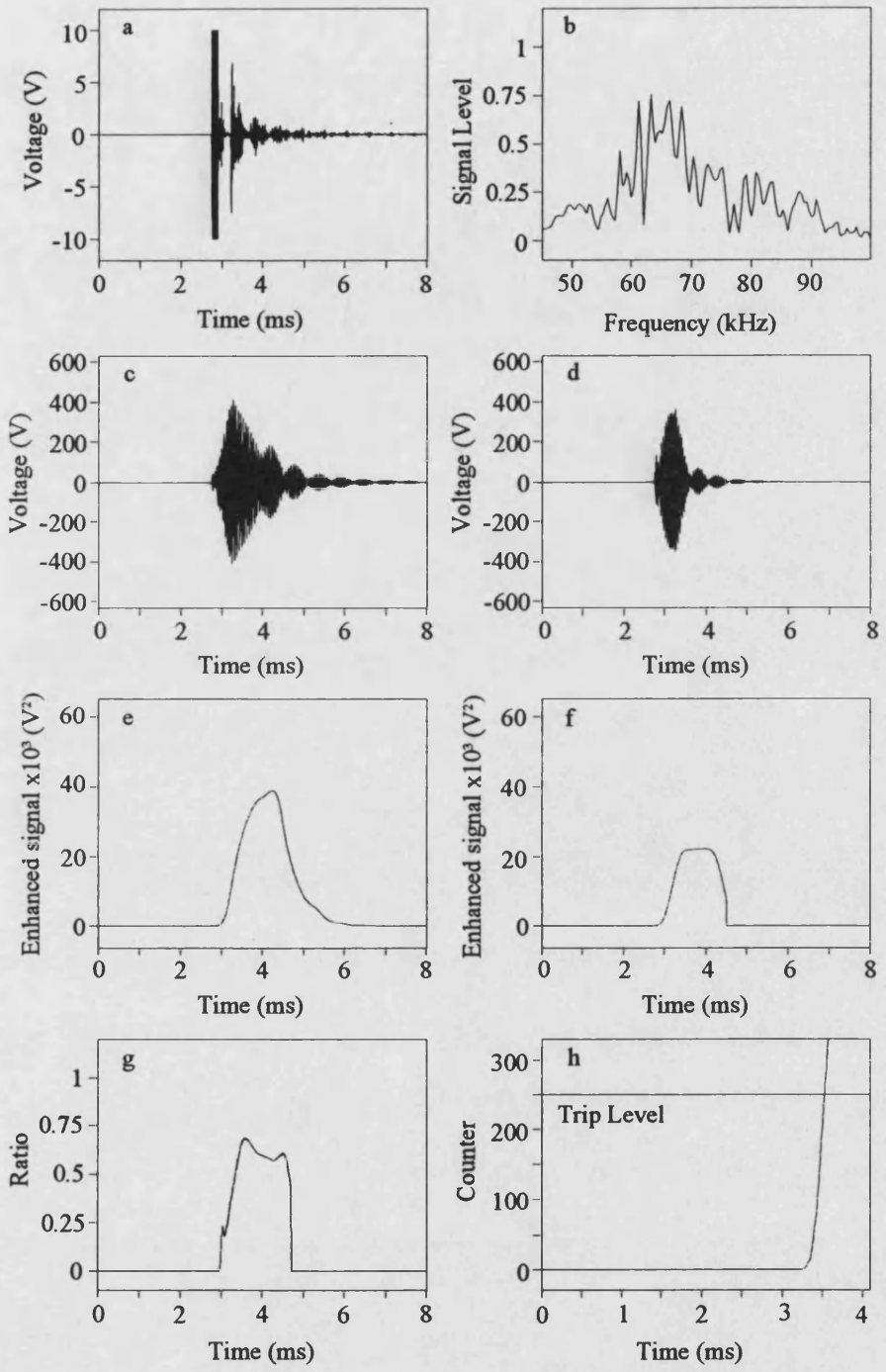
Fig. 7.5 - Plain circuit end P internal fault response



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

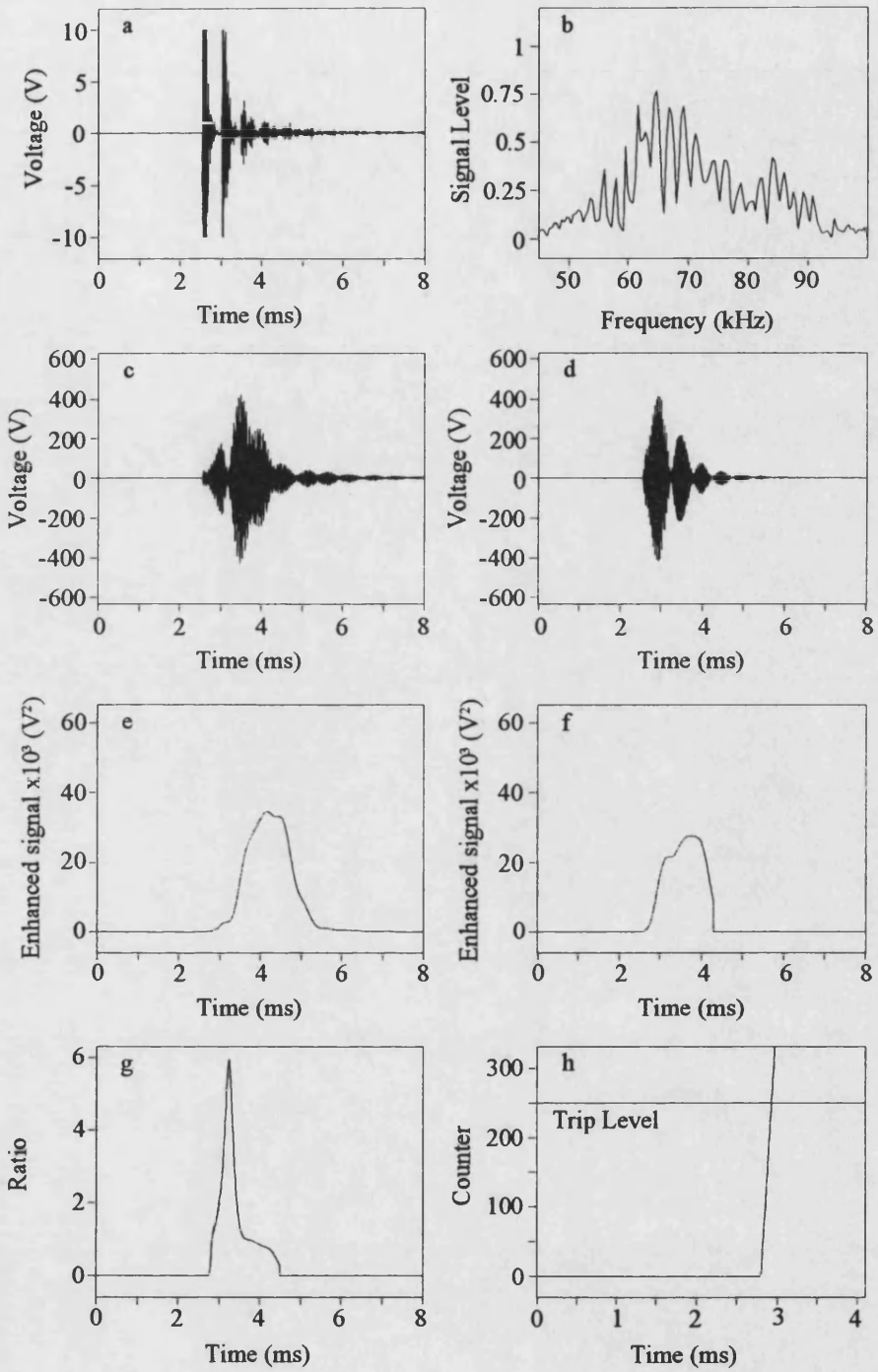
Fig. 7.6 - Plain circuit end Q internal fault response



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

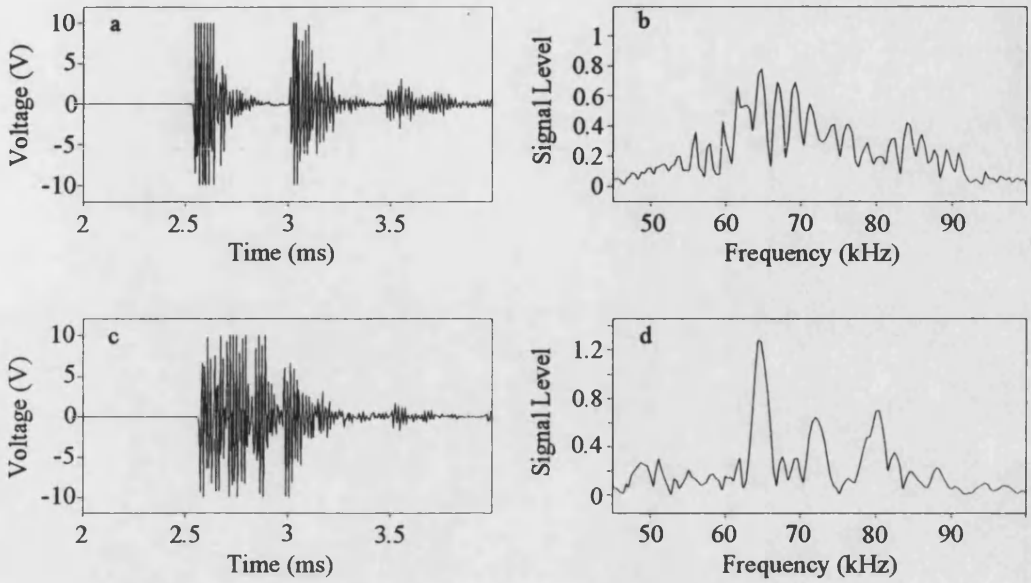
Fig. 7.7 - Composite circuit 1 end P internal fault response



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 7.8 - Composite circuit 1 end Q internal fault response



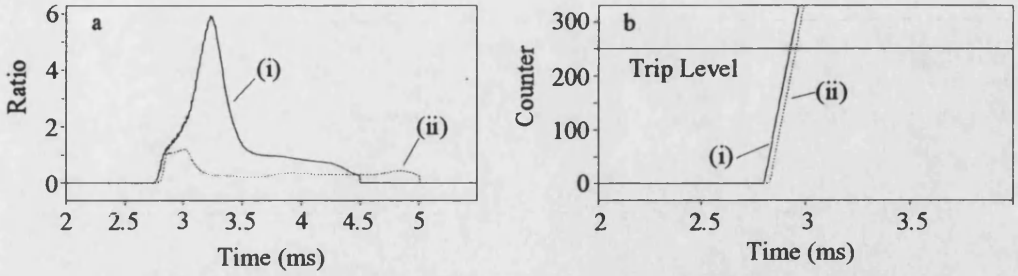
Plain network : a End Q stack tuner output b Frequency spectrum of a

Composite circuit 1 : c End Q stack tuner output d Frequency spectrum of c

Fault inception, $t_f = 2.5$ ms

Fig. 7.9 - End Q stack tuner responses

The discrimination ratio at end Q reaches approximately one on the composite circuit and peaks at just below six on the plain circuit (Fig. 7.10a). The trip levels are exceeded less than 0.5 ms after fault inception and a correct internal fault decision is made in both cases (Fig. 7.10b). The composite network decision is only slightly slower than the plain network because of the slower travel times through the cable. The additional distortion does not affect the correct performance of the scheme.



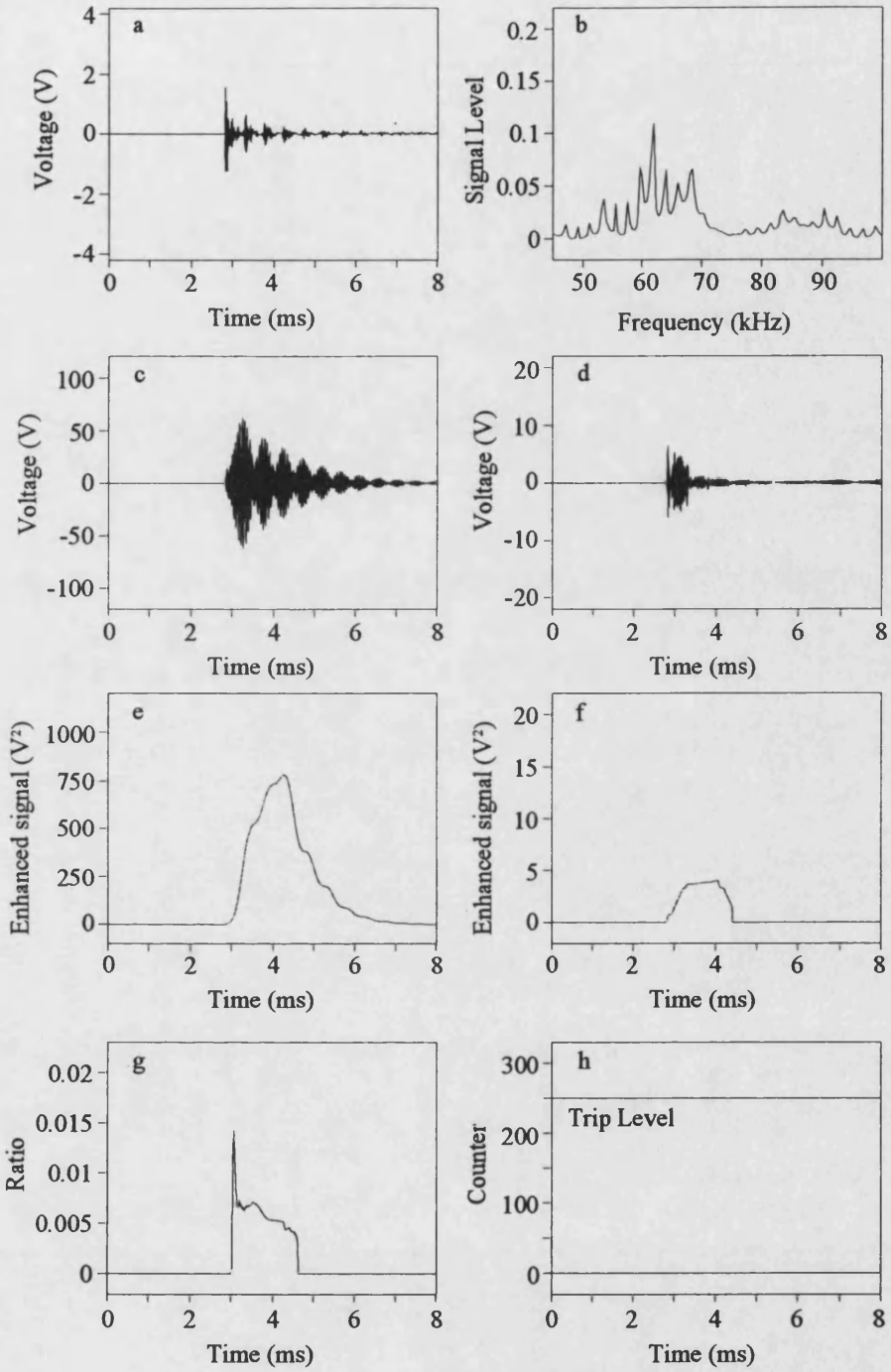
a End Q discrimination ratios

b End Q trip counter outputs

(i) Plain network (ii) Composite circuit 1

Fig. 7.10 - Internal fault trip decisions

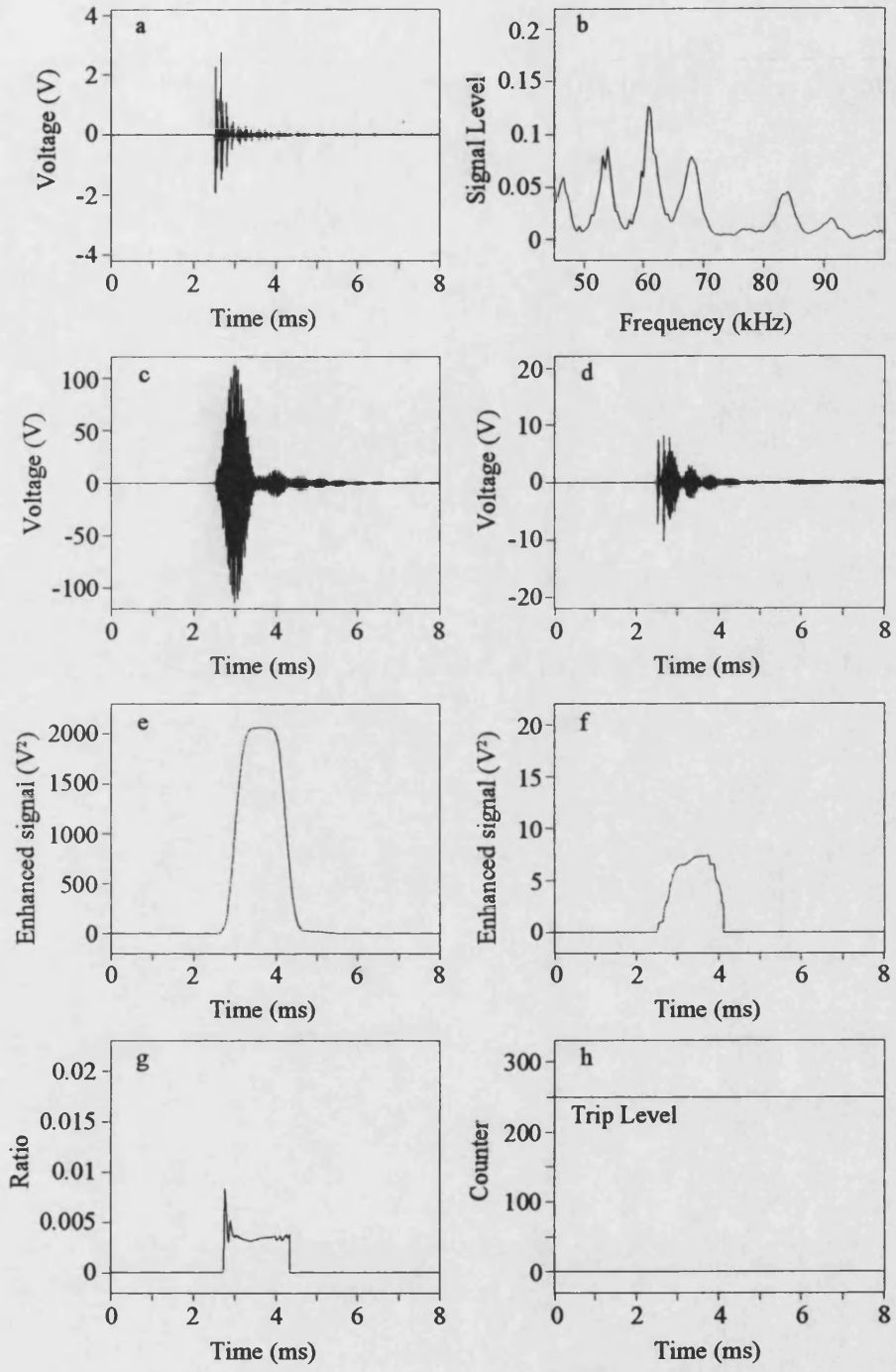
Similar characteristics can also be seen in an external fault case. Here a -5° phase b to earth fault is applied at end Q on the plain network and on composite circuit 1 (point F_{19} and F_{21}). Figures 7.11-7.14 show all of the mode V_x waveforms for the two faults. Examining the end Q signals more closely, it can be seen that the noise bursts visible on the stack tuner outputs for the first case, are primarily due to reflections from the remote end, P (Fig. 7.15a). The frequency spectrum of this waveform clearly shows the blocking effect of the line trap (Fig. 7.15b). On composite circuit 1, the majority of the reflections are from the underground cable and overhead line interface (Fig. 7.15c). The cable distortion can be seen in the frequency domain but there is still significant attenuation around the tuned frequency band (Fig. 7.15d). Therefore, both of these give rise to a very low discrimination ratio, less than 0.02 (Fig. 7.15e), and so the trip counters remain at zero (Fig. 7.15f) and so the algorithm remains stable.



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

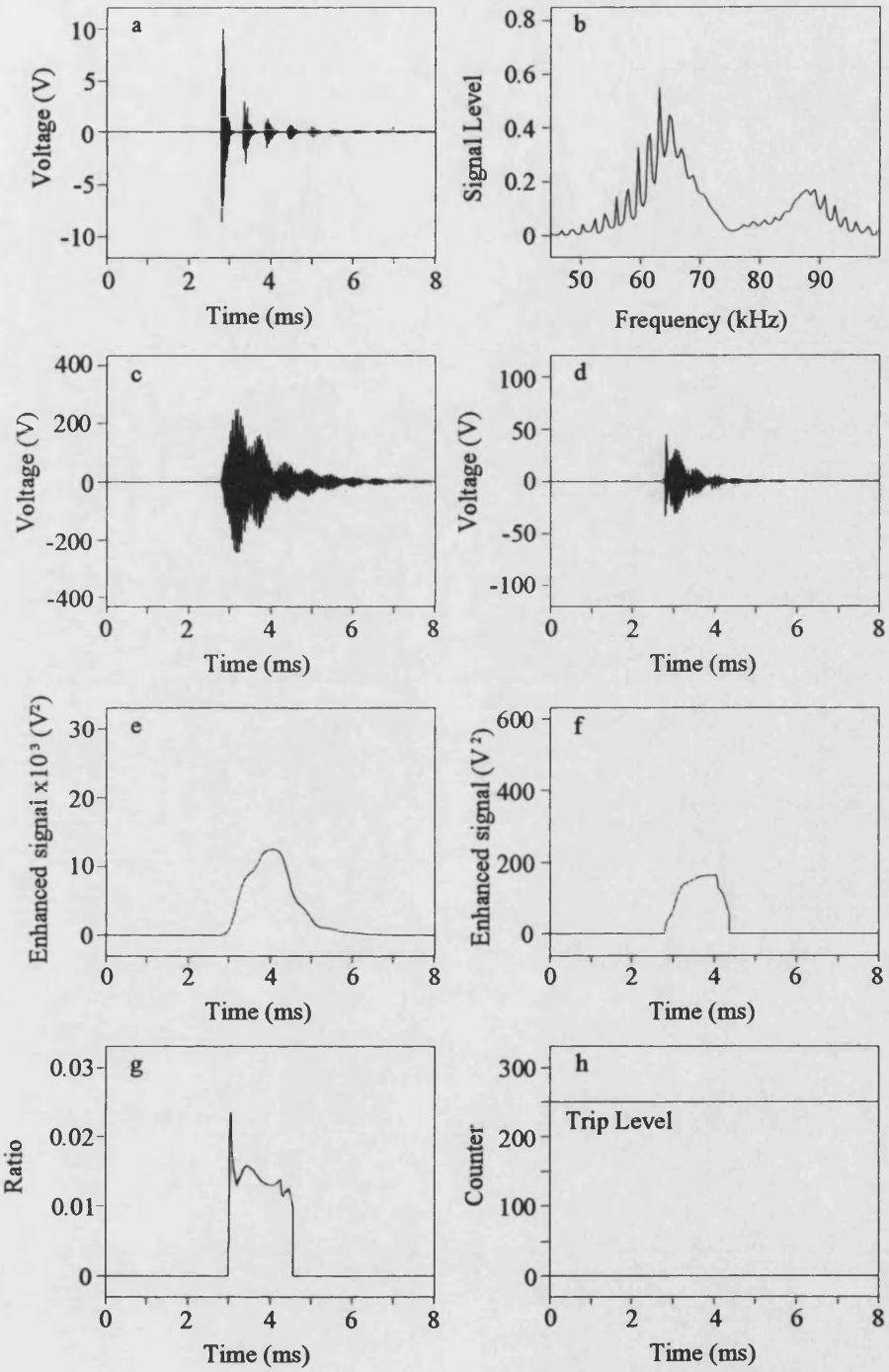
Fig. 7.11 - Plain circuit end P external fault response



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

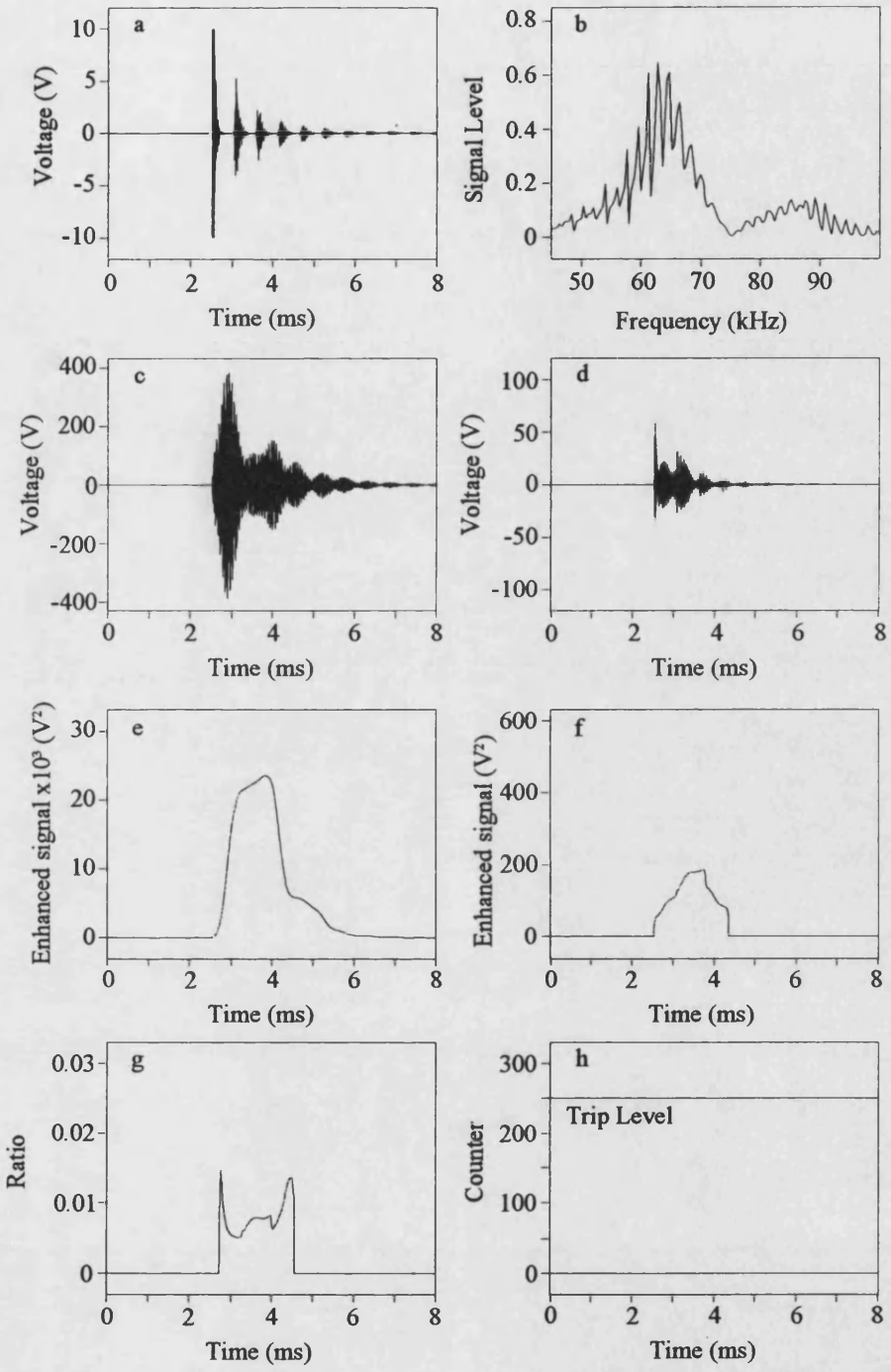
Fig. 7.12 - Plain circuit end Q external fault response



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

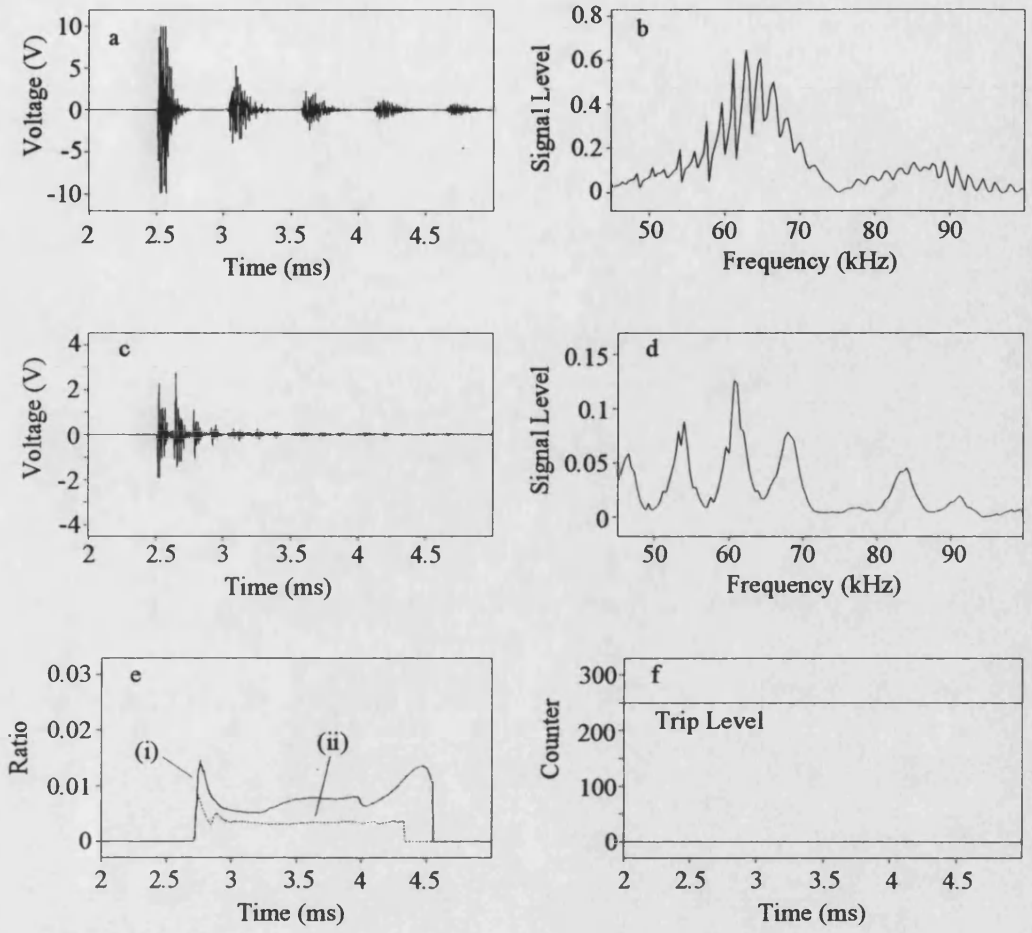
Fig. 7.13 - Composite circuit 1 end P external fault response



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 7.14 - Composite circuit 1 end Q external fault response



Plain network : a End Q stack tuner output b Frequency spectrum of a

Composite circuit 1 : c End Q stack tuner output d Frequency spectrum of c

e End Q discrimination ratios f End Q trip counter outputs

(i) Plain network (ii) Composite circuit 1

Fault inception, $t_f = 2.5$ ms

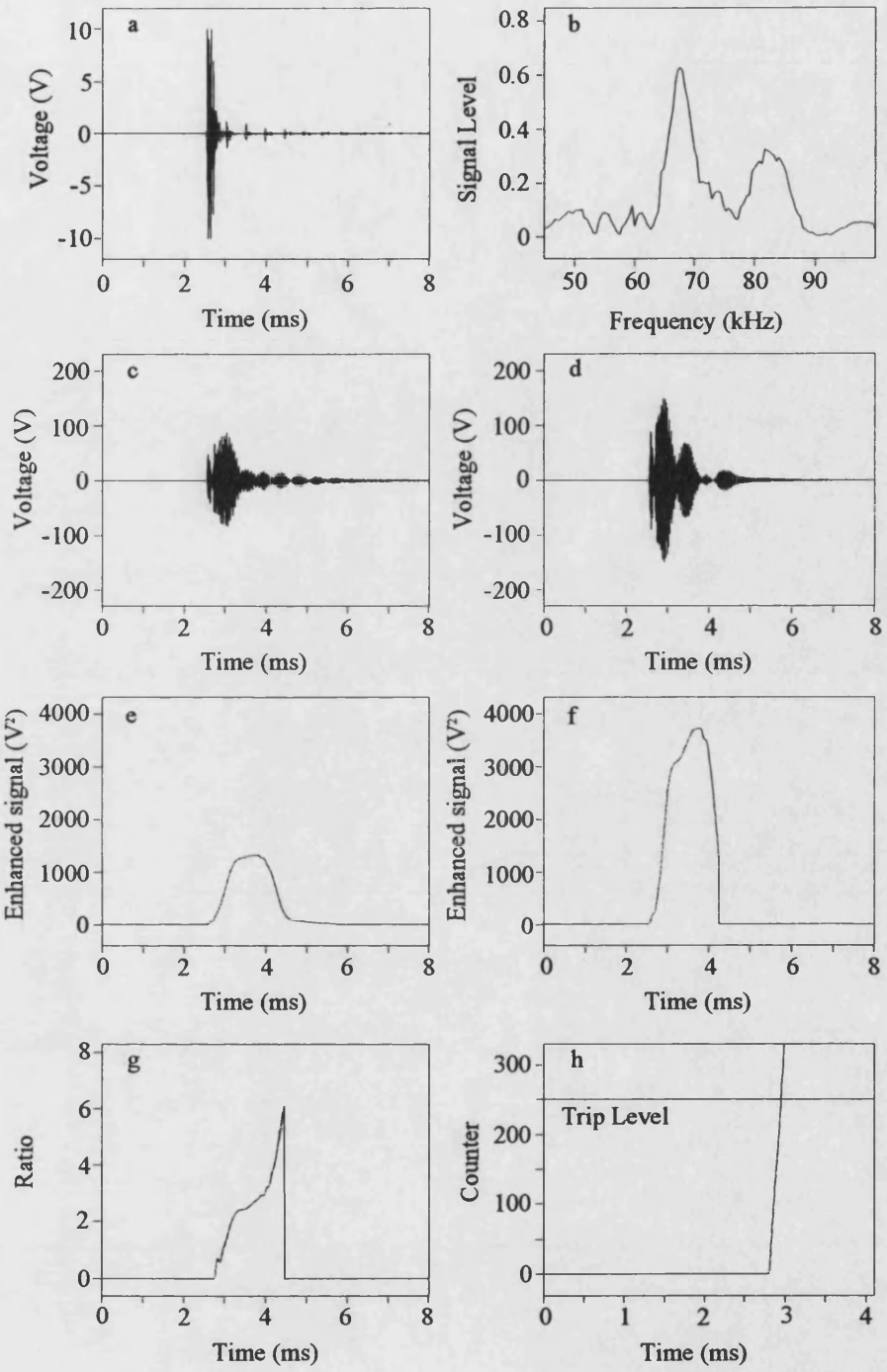
Fig. 7.15 - End Q responses

A selection of internal and external were applied to cable circuits 2 and 3 and a summary of their results are shown in Table 7.6. Again the relay performs correctly and gives the necessary trip output in approximately one millisecond. The mode V_x waveforms for the phase b to phase c fault at F_{22} at ends P and Q are shown in Figs. 7.16 and 7.17 respectively. Figures 7.18 and 7.19 show the mode V_y responses at both ends for the three phase fault at F_{25}.

Table 7.6 - Composite circuit performance

N/O - No Operation

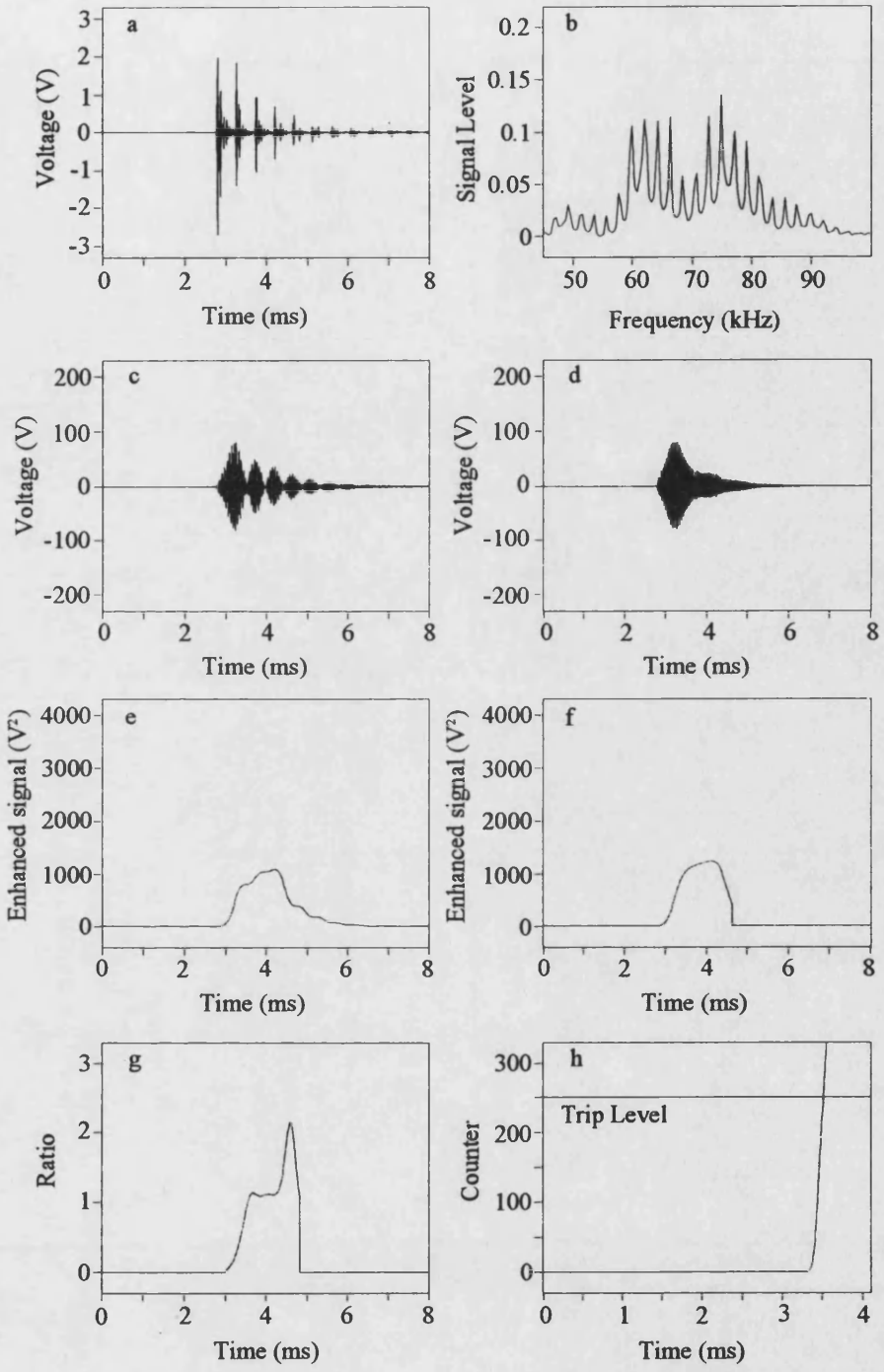
Fault characteristics Note: Fault angle is the angle of V_a at end P			Time to trip after fault inception (ms)			
			End P		End Q	
Position	Angle	Type	Mode V_x	Mode V_y	Mode V_x	Mode V_y
F_{22}	10°	BC	0.45	0.46	1.015	1.02
F_{23}	105°	ABC-E	N/O	N/O	N/O	N/O
F_{24}	35°	CA-E	0.875	0.705	0.585	0.885
F_{25}	-60°	ABC	N/O	N/O	N/O	N/O



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

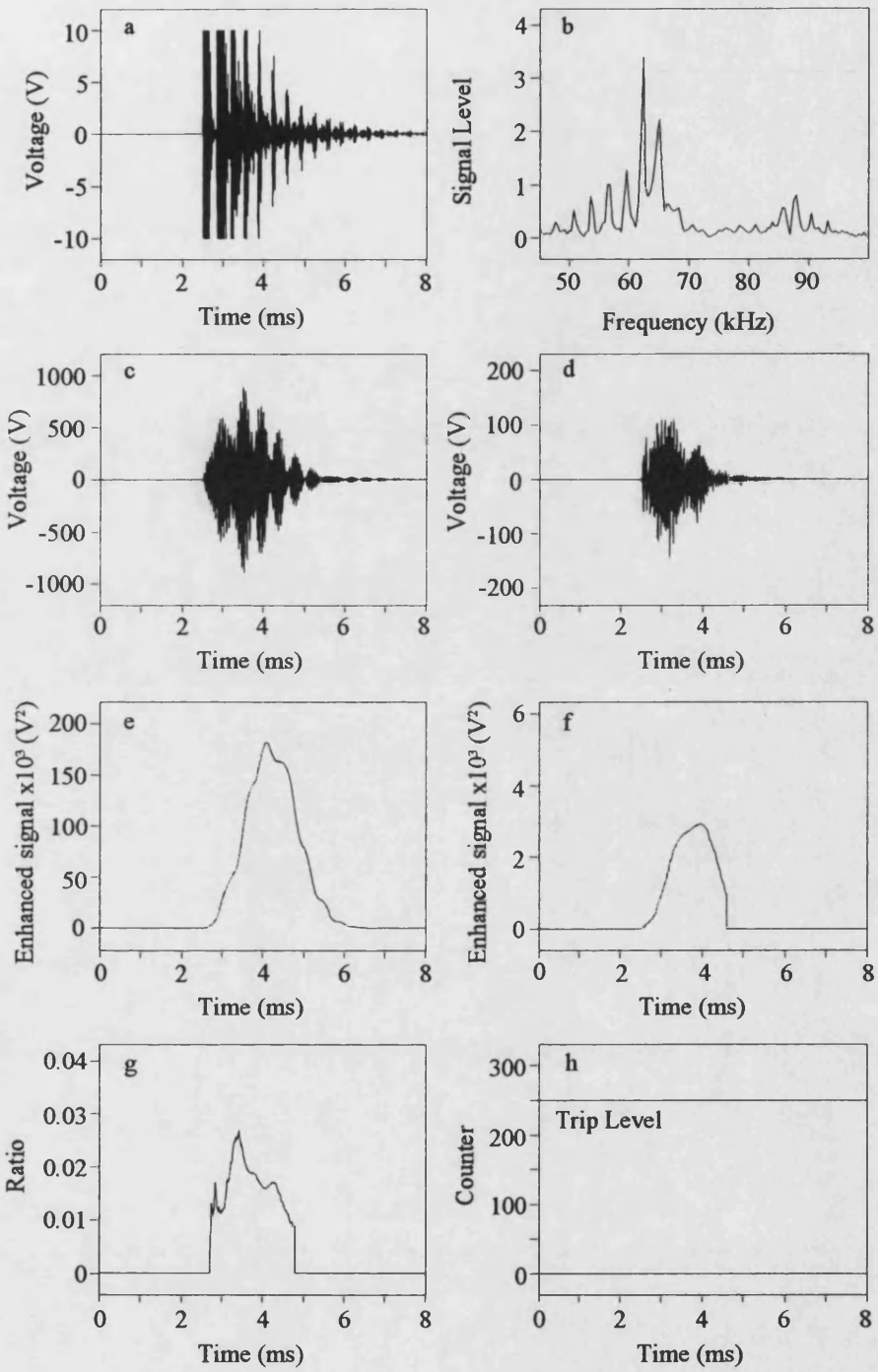
Fig. 7.16 - Internal fault at F_{22} mode V_x response at end P



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

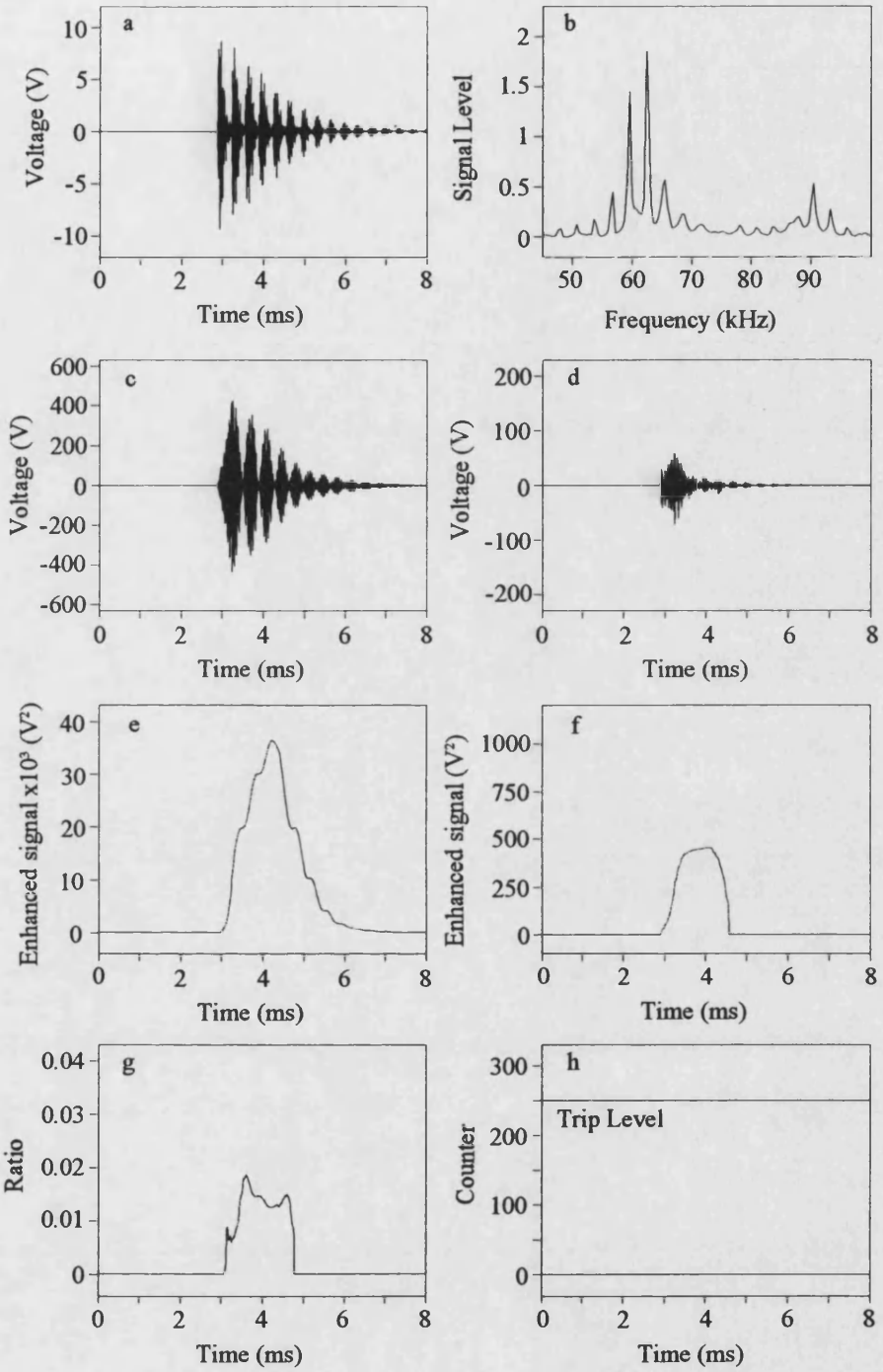
Fig. 7.17 - Internal fault at F_{22} mode V_x response at end Q



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 7.18 - External fault at F_{25} mode V_y response at end P



a Stack tuner output
b Frequency spectrum of a
c Restraint filter output
d Operate filter output
e Enhanced restraint filter output
f Enhanced operate filter output
g Discrimination ratio
h Trip counter output

Fault inception, $t_f = 2.5$ ms

Fig. 7.19 - External fault at F_{25} mode V_y response at end Q

CHAPTER 8

CONCLUSIONS AND FURTHER WORK

8.1 Summary of Work

This thesis presents a technique for protecting complex EHV circuits by using the high frequency signals generated by arcing faults. The signals are captured with specially designed stack tuner circuits which are connected to each phase via the coupling capacitor of standard capacitor voltage transformers. The three phase signals are combined to form two modal signals which are fed into a signal processing unit. This removes the common mode which minimises any mutual coupling effects. Digital filters are used to extract the necessary information from these signals. The filter outputs are enhanced to give a measure of their spectral power and are then compared to give a discrimination ratio. This ratio is used with some carefully designed decision logic to determine whether a fault is internal or external to the protected zone.

The boundary of the zone to be protected is marked by PLC line traps. The bandstop nature of the line traps give the high frequency signals distinct characteristics which enables the discrimination between internal and external faults to be achieved. HF signals originating from outside the protected zone will have a narrow band of

frequencies around the centre frequency of the line traps severely attenuated. Signals originating inside the zone, however, will not have passed through the line traps and so the narrow frequency band around the centre frequency will be present.

A number of different power system networks have been simulated using the EMTP. The simulations contain a primary arc model which takes into account the time varying behaviour of the electric arc. Single circuit 400 kV overhead transmission lines have been modelled with frequency dependent parameters along with a typical underground cable configuration.

8.2 Conclusions

The results show that the relay can clearly distinguish between internal and external faults on a wide variety of EHV teed and composite circuits. It is not adversely affected by different fault positions or types and can cope with very high fault resistances. At each line terminal, the line trap and busbar stray capacitance form a very high impedance barrier to the high frequencies around the line trap centre frequency. This means that the scheme is insensitive to the capacities of the connected sources and it is immune to any problems caused by line loading.

The technique has the discriminative properties normally associated with unit protection but it only uses locally derived information. Therefore, it does not need expensive communication channels which, if they fail, can have serious effects on the performance of some other protection techniques. It also does not rely on the actual

magnitudes of the detected signals once a minimum threshold level has been exceeded. This is because the discrimination ratio, which is central to the techniques operation, is formed from a comparison of the relative strengths of two signals which are each centred on a narrow band of frequencies. The HF signals that are captured by the stack tuners have a very large dynamic range and so they have to be limited before they can be digitised. This clipping procedure does not affect the scheme's ability to discriminate between internal and external faults.

A sensitivity analysis has demonstrated that this method is stable for slight parameter variations that might be encountered in practice. Carefully designed decision logic adds further security to the scheme by ensuring that a trip decision is only given when the discrimination ratio remains high for a significant length of time. No setting of the relay is required for individual circuit arrangements once the operate and restraint filter centre frequencies have been fixed. These are predetermined by the type of network being protected, ie a teed, or a composite circuit. This eliminates any problems that could arise from the relay being incorrectly set.

Computer simulations have shown that correct trip decisions can be made for all fault types in approximately one millisecond. The simulations and subsequent calculations are performed off-line and so do not take into account any delays due to the analogue processing or the time taken for the processors to perform the necessary calculations. It is envisaged that a hardware implementation of this relay would use high performance floating point parallel processors. The total operating time of the protection relay using these processors is still estimated to be under five milliseconds.

8.3 Further Work

All of the work in this thesis has been computer simulated and so the next stage is to build a prototype relay. It has been calculated that four Texas Instruments TMS320C40 parallel processors would be able to perform all of the necessary calculations within the 5 μs sampling interval. A prototype could therefore be constructed using these devices and then tested to ensure that it is capable of working in real time.

The testing could be performed using three different types of signals: simulated data; prerecorded data; and actual real time data. Both the simulated data and the prerecorded data could be fed into the relay at two different levels. The easiest is to supply digital data directly into the prototype relay at a digital level. This, however, bypasses the analogue processing and the A/D conversion process and so any delays or other disturbances caused by these sections will not be taken into account. These two sections could be tested if the digital data were used to produce time domain analogue waveforms. This would involve constructing a piece of hardware that was capable of supplying the signals at suitable voltage and current levels. This would provide more comprehensive testing of the relay.

The simulated data would enable the prototype to be tested for a very large number of fault conditions and situations that may be encountered in practice. The prerecorded data has the advantage that it is from a real situation and so would include some typical background and random noise on the signals. The data would have had

to have been captured with at least a 200 kHz sampling rate for it to contain the necessary information. This data is likely to have come from a limited number of tests and so may not have the variety of the simulated data. Using a combination of simulated and prerecorded data would therefore provide the prototype with fairly thorough testing.

The final testing procedure would involve using actual real time data. This would mean installing the prototype relay at a substation and supplying it directly from the stack tuner output in a field trial. This is, of course, the most comprehensive test environment but it is very expensive and has a number of potential problems. It initially relies on finding a suitable test circuit (ie a teed or a composite circuit) with an electricity transmission company who is willing to co-operate. Once this has been done, there is no guarantee that any useful data would be recorded as faults are random in nature and so their time and position cannot be predicted. It is possible that the circuit being monitored might not experience any actual faults during the timescale of the field trial. However, this is still the most complete way of testing a prototype relay as it subjects it to the exact situation that it would encounter in practice.

CHAPTER 9

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APPENDIX

PUBLISHED WORK

The following papers are based on the work covered in this thesis and are included for reference.

1. A. M. CARTER, Z. Q. BO, R. K. AGGARWAL, A. T. JOHNS, 'Measurement of fault generated high frequency noise on teed transmission systems', 28th Universities Power Engineering Conference, Staffordshire University, September 1993
2. A. M. CARTER, Z. Q. BO, R. K. AGGARWAL, A. T. JOHNS, 'A novel non-unit protection scheme for EHV teed transmission circuits using fault generated high frequency noise', Conference on Developments in Power System Protection and Local Control, Beijing, China, May 1994
3. A. M. CARTER, R. K. AGGARWAL, A. T. JOHNS, Z. Q. BO, 'Non-unit protection of EHV composite circuits based on fault generated high-frequency noise', provisionally accepted for 3rd IEE Int. Conf., APSCOM, Hong Kong, November 1995
4. A. M. CARTER, R. K. AGGARWAL, A. T. JOHNS, Z. Q. BO, 'Computer-aided design of a new high speed non-unit protection relay for EHV teed circuits', provisionally accepted for publication in IEE Proc. Gen. Tran. Dist.

MEASUREMENT OF FAULT GENERATED HIGH FREQUENCY NOISE ON TEED TRANSMISSION SYSTEMS

A.M.Carter Z.Q.Bo R.K.Aggarwal A.T.Johns

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1.0 INTRODUCTION

Following a sudden change in the system voltage on a transmission network, caused by an arcing fault for example, wide band high frequency noise signals are generated on the associated EHV power lines. These signals are generally outside the bandwidth of most conventional voltage transducers. It has recently been suggested that these signals could be used very effectively to produce new types of protection schemes that would have many advantages over existing power frequency measurement based methods.

A recent paper [1] has shown that wide-band fault generated high frequency noise signals can be captured using capacitor voltage transformers (CVTs) and conventionally connected power line carrier communication signal line traps. The high voltage capacitor of the CVT is used in conjunction with a specially designed stack tuner to capture the signals, whilst the line traps are used to confine the signals to the protected zone.

This paper applies this new technique to the protection of teed transmission line circuits which are now generally regarded as having significant environmental and economic advantages over plain feeders. It shows the effect of fault inception angle and fault position on the high frequency signals detected by the stack tuners and how the discrimination between internal and external faults can be achieved by using frequency spectrum analysis. The paper then goes on to show how the fault generated high frequency noise technique can cope with some of the difficult protection problems associated with teed circuits.

2.0 TEED TRANSMISSION CIRCUITS

Teed circuits are starting to be used more widely due to their often significant economic and also environmental advantages over two terminal transmission lines. However, teed circuits can create some problems for conventional protection schemes that may affect system security [2].

The tee point impedance discontinuity has a major effect on the voltage and current waveforms due to the reflections of travelling waves from this point, as well as from the line terminations and the fault point [3]. Line loading limitations and problems setting the reach of distance protection devices relative to the tee point can also be encountered. Many of these problems are often compounded if the distances from the ends of the transmission lines to the tee point are significantly different.

Another problem associated with teed circuits concerns what are known as 'feed around paths'. Here an external transmission circuit connects two ends of the protected teed network. Certain internal fault conditions cause the current to flow out of one terminal to the terminal closest to the fault via the feed around path. This can make the fault appear to be external to many conventional protection schemes.

3.0 POWER SYSTEM SIMULATION

The simulation of the power system is done using the well proven Electromagnetic Transient Program (EMTP). This contains mathematical models of the power system components allowing the behaviour of different network configurations to be studied under various fault conditions. The program also contains a subsection known as TACS (Transient Analysis of Control Systems) which allows control systems to be modelled and interact directly with the simulations being run within the EMTP. The power system is simulated using the EMTP with a primary electric fault arc being modelled using TACS.

3.1 PRIMARY ARC MODEL

Following a fault, an electric arc develops which is frequently across the line insulators. From the time of the fault to when the circuit breakers open it is known as the primary arc and this becomes a secondary arc once the circuit breakers have opened isolating the line. This paper is only concerned with what happens during the primary arcing time.

In this paper an arc model is used which is derived from the viewpoint of control system theory on the energy balance of the arc column first developed by Hochrainer [4,5] which is based on switching arc theory. It can be written as

$$\frac{dg}{dt} = \frac{1}{\tau}(G - g) \qquad (1)$$

where

g - time varying arc conductance
G - stationary arc conductance
τ - time constant

This allows the dynamic behaviour of the arc to be described. The stationary arc conductance, G can be physically interpreted as the arc conductance value that would set in if the current were maintained under constant external conditions for a sufficiently long time and can evaluated from

$$G = \frac{|I|}{(V_o + R|I|)l} \qquad (2)$$

where

I - arc current
V_o - constant voltage parameter per unit arc length
R - resistive component per unit arc length
l - time dependant arc length

The time varying arc conductance is calculated by solving the arc equation (1) at each time step using the following equation (3) making the assumption that the stationary arc conductance and time constant remain constant during each time step.

$$g(t) = G(t-\Delta t) - [G(t-\Delta t) - g(t-\Delta t)]\exp(-\Delta t/\tau) \qquad (3)$$

The reciprocal of this then gives the time varying arc resistance.

The electrical network and the control system (arc model) are solved separately within the EMTP and TACS respectively at each time step using the data from the previous time step. The simulation is always started from the steady state condition.

4.0 NETWORK CONFIGURATION

The transmission lines modelled in this simulation are based on a single circuit of the typical quad-conductor 400 kV vertical construction line currently used on the UK supergrid system [6]. The frequency dependence of the line parameters are simulated using the J.Marti line model within the EMTP. A system frequency of 50 Hz and an earth resistivity of 100 Ωm are also used.

The two different network configurations that were studied are shown in Figure 1. Figure 1(a) shows a symmetrical tee with equal source capacities and Figure 1(b) is an unsymmetrical tee with a feed around path and unequal source capacities.

4.1 SOURCE CONFIGURATION

The source X/R ratio is taken to be 30 and a shunt busbar capacitance of 0.1 μF is assumed at each terminating

busbar. Connected between the source and the outgoing transmission line at each terminal is the line trap and stack tuner arrangement. This is shown in Figure 2.

The line trap is the standard type used in power line carrier applications and can be tuned to block a narrow band of high frequencies (i.e. a high impedance) whilst appearing to be a very low impedance at all other frequencies. Using parameters obtained from the National Grid Company, the line traps were tuned to a centre frequency of 100 kHz and a frequency range of 90 - 110 kHz.

The stack tuner is connected to the transmission line via the coupling capacitor of a standard CVT. It consists of a series tuning inductor L_s and a parallel RLC network tuned the centre frequency of 100 kHz. The stack tuner is arranged so that it has a very high impedance at the power frequency (50 Hz) and is close to the line characteristic impedance at the tuned frequency (100 kHz). This is to minimise the attenuation at the tee point [7].

The line trap / stack tuner arrangement shown in Figure 2 is connected to each of the three phases at each end of the teed circuit to be protected.

5.0 BASIC PROTECTION STRATEGY

A fault on the power system will cause wideband high frequency noise to be generated which will travel rapidly through the network due to the high propagation velocity of the travelling waves (slightly less than the speed of light). If the fault is internal to the network being protected there will be a relatively consistent signal around 100 kHz from the output of the stack tuner. If the fault is external then there will be severe attenuation of a very small band of high frequencies around the tuned frequency (100 kHz) due to the presence of the line trap and the busbar capacitance. This will be shown more clearly later on in this paper.

6.0 SIMULATION RESULTS

A number of studies were carried out at different fault inception angles and different fault points to represent both internal and external fault conditions. The results presented in this paper are only for single phase to earth faults (as these are the most commonly occurring) and the outputs are for the faulted phase only. The fault is applied after 2.5 ms.

Figure 3 shows the results for a fault 40 km from end P on the symmetrical tee network of Figure 1(a) occurring at voltage maximum. The signals detected by the stack tuners at ends P and Q , Figure 3(a)&(b), are very similar except the attenuation of the line and tee point reduces the magnitude of the signals detected at end Q. The periodic bursts of noise occurring after the initial fault inception are due to the non-linear nature of the fault arc path particularly when it is close to a current zero. This distorting effect on the voltage at the fault point is shown in Figure 3(c). Frequency spectra of the stack tuner outputs, Figure 3(d)&(e), show a fairly strong wide band of frequencies around 100 kHz.

Figure 4 shows the results for a fault inception angle of 0^o at the same position as before. The stack tuner outputs, Figure 4(a)&(b), are again similar with an initial noise burst at fault inception and subsequent bursts which this time are not periodic due to the dc offset of the current waveform. The frequency spectra, Figure 4(c)&(d) again show a fairly wide band of frequencies around the tuned frequency of 100kHz. This indicates that the high frequency noise signals are present for all fault inception angles.

For a single phase to ground fault on the busbar at end P just behind the line trap, i.e. external to the protected circuit, the stack tuner outputs, Figure 5(a)&(b), appear to be similar to the internal fault condition in the time domain. However, in the frequency domain, Figure 5(c)&(d), it can be clearly seen that the high frequencies around 100 kHz are severely attenuated. This is directly due to the presence of the line trap which causes these signals to be shunted to ground via the busbar shunt capacitance. A comparison of the internal and external fault frequency spectra shows that correct protection discrimination can be achieved.

Figure 6 demonstrates how the new technique can cope with the feed around path problem. An internal fault was applied 10 km from end P on the unsymmetrical tee circuit of Figure 1(b) at a fault inception angle of 0^o. The current waveforms at each end, Figure 6(a)(b)&(c), clearly show the outfeed condition from end R. This is due to the fault current flowing via the feed around path which could confuse conventional protection schemes. The frequency spectra of the stack tuner outputs, Figure 6(d)(e)&(f) all show a consistent band of frequencies around the centre frequency which indicates an internal fault condition.

The line loading problem was examined by varying the power transfer angle between the three ends of the circuit. This was found not to have a significant effect on the nature of the signals detected by the stack tuners.

7.0 CONCLUSIONS

This paper shows how a new protection concept, based on power line carrier communication techniques, can be used to protect teed circuits. It is not adversely affected by the fault inception angle and can discriminate between internal and external faults even in the presence of a feed around path.

8.0 ACKNOWLEDGEMENTS

The authors are grateful for the financial support of the SERC and NGC, and the University of Bath for the provision of facilities.

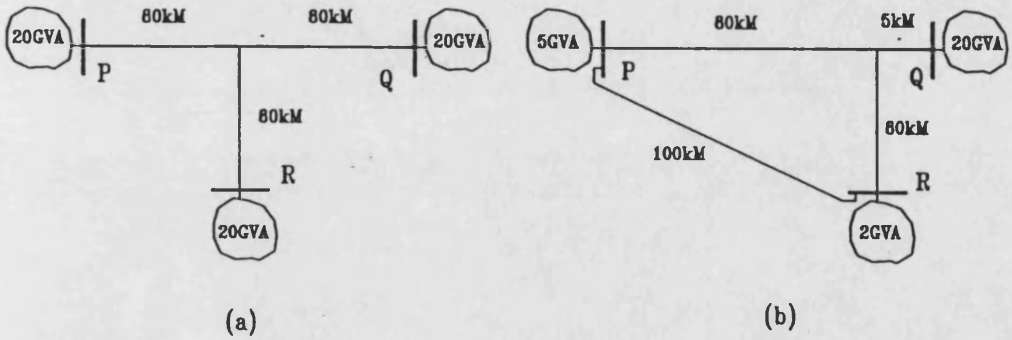

Fig 1 – Network Configurations

9.0 REFERENCES

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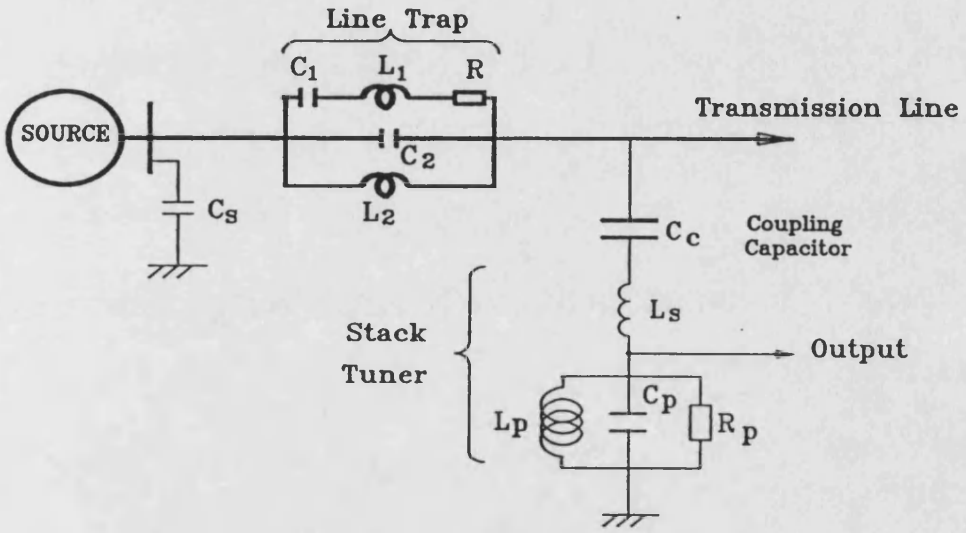
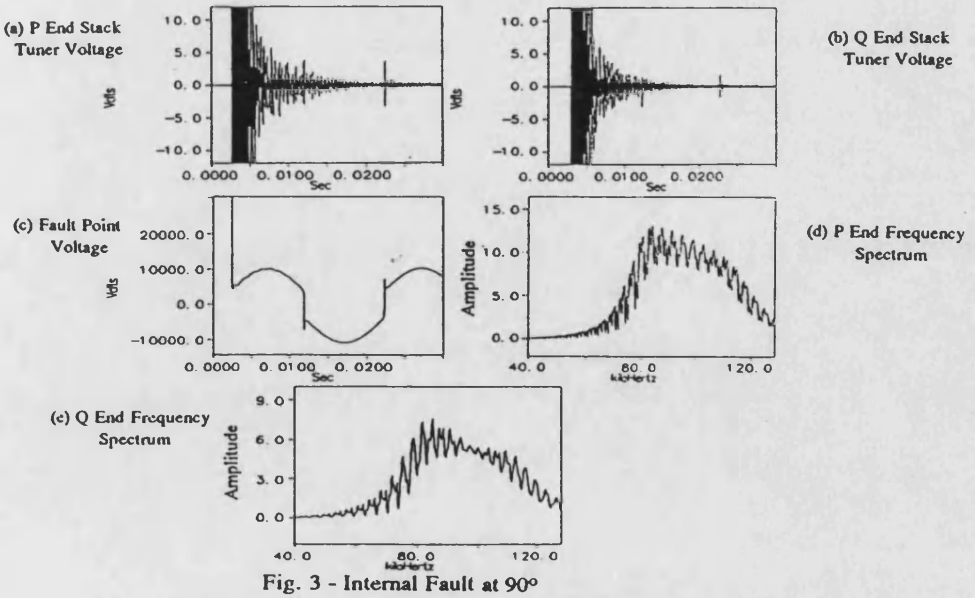


Fig 2 – Line Trap / Stack Tuner Arrangement



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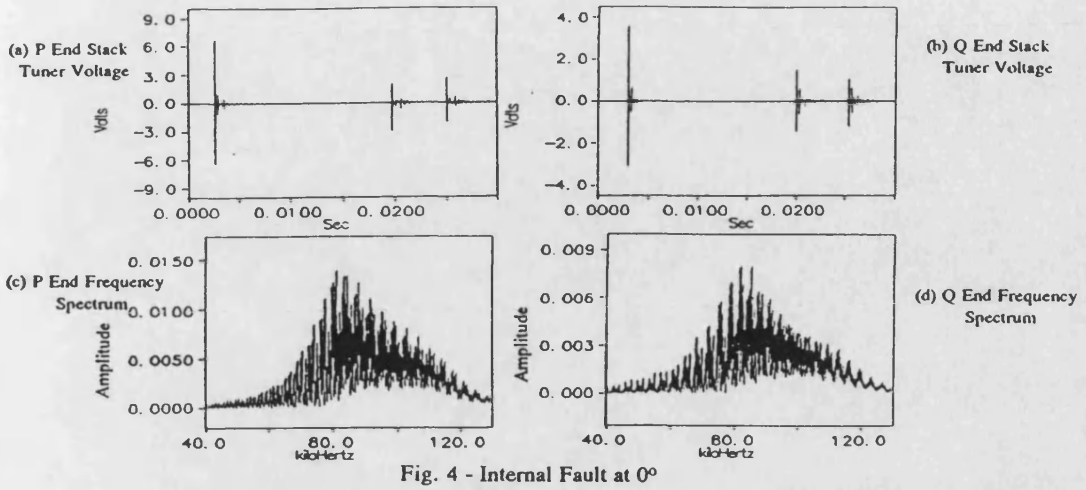

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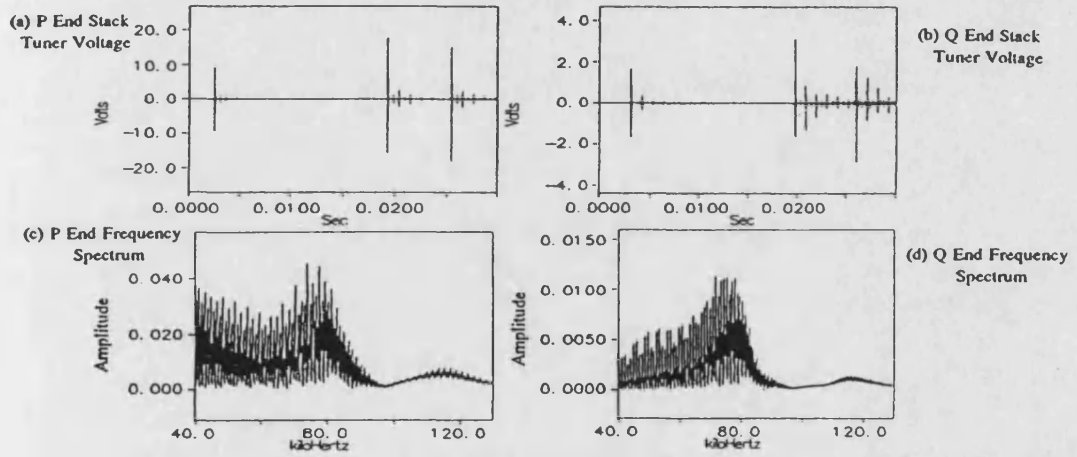

Fig. 5 - External Fault at 0°

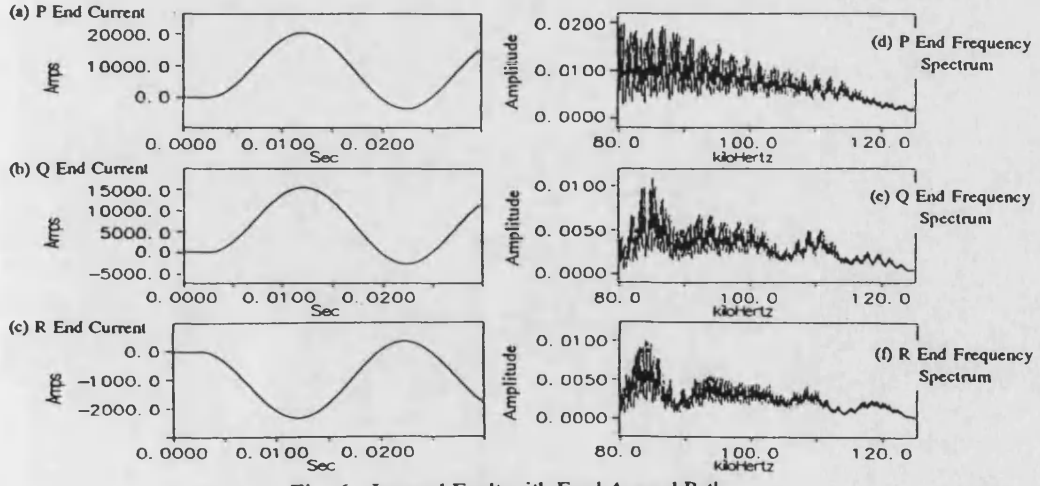

Fig. 6 - Internal Fault with Feed Around Path

A NOVEL NON-UNIT PROTECTION SCHEME FOR EHV TEED TRANSMISSION CIRCUITS USING FAULT GENERATED HIGH FREQUENCY NOISE

A.M.Carter Z.Q.Bo R.K.Aggarwal A.T.Johns

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Abstract. The use of fault generated high frequency noise to produce a novel non-unit protection scheme is discussed. The high frequency signals are captured using a capacitor voltage transformer and a specially designed stack tuner. Conventionally power line communication signal line traps are used to confine the high frequency noise signals to the protected zone. This technique is applied to the protection of teed EHV transmission circuits, which are starting to be used more widely but they can have some protection problems which may affect system security. The simulated results show that the technique is capable of discriminating between internal and external faults and is not adversely affected by the fault inception angle, line loading or feed around paths.

INTRODUCTION

Wide-band high frequency noise signals are generated by arcing faults. These signals are generally outside the band-width of most conventional voltage transducers. It has recently been suggested that these signals could be used very effectively to produce new types of protection schemes that would have many advantages over existing power frequency based methods.

A recent paper (Bo, Aggarwal and Johns,1992) has shown that wide-band fault generated high frequency noise signals can be captured using capacitor voltage transformers (CVTs) and conventionally connected power line carrier communication signal line traps. The high voltage capacitor of the CVT is used in conjunction with a specially designed stack tuner to capture the signals, whilst the line traps are used to confine the signals to the protected zone.

Teed circuits are starting to be used more widely due to their often significant economic and also environmental advantages over two terminal transmission lines. However, teed circuits can create some problems for conventional protection schemes that may affect system security (IEE Power Systems Relaying Committee,1979).

The tee point impedance discontinuity has a major effect on the voltage and current waveforms due to the reflections of travelling waves from this point, as well as from the line terminations and the fault point (Rajendra and McLaren,1985). Line loading limitations and problems setting the reach of distance protection devices relative to the tee point can also be encountered. Many of these problems are often compounded if the distances from the ends of the transmission lines to the tee point are significantly different.

Another problem associated with teed circuits concerns what are known as 'feed around paths'. Here an external transmission circuit connects two ends of the protected teed network. Certain internal fault conditions cause the current to flow out of one terminal to the terminal closest to the fault via the feed around path. This can make the fault appear to be external to many conventional protection schemes.

This paper applies this new technique to the protection of teed transmission line circuits. It shows the effect of fault inception angle and fault position on the high frequency signals detected by the stack tuners and how the discrimination between internal and external faults can be achieved by using frequency spectrum analysis. The paper then goes on to show how the fault generated high frequency noise technique can cope with some of the difficult protection problems associated with teed circuits.

POWER SYSTEM SIMULATION

The simulation of the power system is done using the well proven Electromagnetic Transient Program (EMTP). This contains mathematical models of the power system components allowing the behaviour of different network configurations to be studied under various fault conditions. Due to the high frequencies involved a simulation rate of 200 kHz is used. The program also contains a subsection known as TACS (Transient Analysis of Control Systems) which allows control systems to be modelled and interact directly with the simulations being run within the EMTP. The power system is simulated using the EMTP, into which a primary electric fault arc model is embodied using TACS.

Primary Arc Model

Following a fault, an electric arc develops which is frequently across the line insulators. The primary arc exists from the time of fault inception to when the circuit breakers open and this becomes a secondary arc once the circuit breakers have opened isolating the line. This paper is only concerned with what happens during the primary arcing time.

In this paper an arc model is used which is derived from the viewpoint of control system theory on the energy balance of the arc column first developed by Hochrainer (Kizilcay and Pniok,1991; Song, Aggarwal and Johns,1992) which is based on switching arc theory.

It can be written as

$$\frac{dg}{dt} = \frac{1}{\tau}(G - g) \qquad (1)$$

where

g	-	time varying arc conductance
G	-	stationary arc conductance
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This allows the dynamic behaviour of the arc to be described. The stationary arc conductance, G can be physically interpreted as the arc conductance value that would set in if the current were maintained under constant external conditions for a sufficiently long time and can evaluated from

$$G = \frac{|I|}{(V_o + R\,|I|)\ell} \qquad (2)$$

where

I	-	arc current
V_o	-	constant voltage parameter per unit arc length
R	-	resistive component per unit arc length
ℓ	-	time dependant arc length

The time varying arc conductance is calculated by solving the arc equation (1) at each time step using the following equation (3) making the assumption that the stationary arc conductance and time constant remain constant during each time step.

$$g(t) = G(t-\Delta t) - [G(t-\Delta t) - g(t-\Delta t)]\exp(\frac{-\Delta t}{\tau}) \qquad (3)$$

The reciprocal of this then gives the time varying arc resistance.

The electrical network and the control system (arc model) are solved separately within the EMTP and TACS respectively at each time step using the data from the previous time step. The simulation is always started from the steady state condition.

NETWORK CONFIGURATION

The transmission lines modelled in this simulation are based on a single circuit of the typical quad-conductor 400 kV vertical construction line currently used on the UK supergrid system (Johns and Aggarwal,1976). The frequency dependence of the line parameters are simulated using the J.Marti line model within the EMTP. A system frequency of 50 Hz and an earth resistivity of 100 Ωm are also used.

The two network configurations that were studied are shown in Fig. 1. Figure 1a shows a symmetrical tee with equal source capacities and Fig. 1b is an unsymmetrical tee with a feed around path and unequal source capacities.

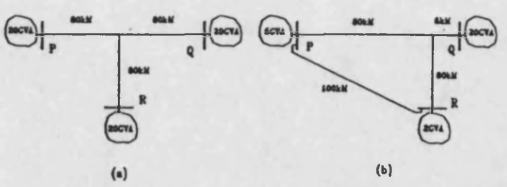


Fig. 1. Network configurations

Source Configuration

The source X/R ratio is taken to be 30 and a shunt busbar capacitance of 0.1 μF is assumed at each terminating busbar. Connected between the source and the outgoing transmission line at each terminal is the line trap and stack tuner arrangement. This is shown in Fig. 2.

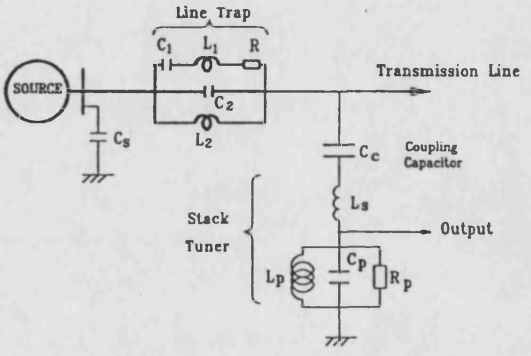


Fig. 2. Stack tuner / line trap arrangement

The line trap is the standard type used in power line carrier applications and can be tuned to block a narrow band of high frequencies (i.e. a high impedance) whilst appearing to be a very low impedance at all other frequencies. Using parameters obtained from the National Grid Company, the line traps were tuned to a centre frequency of 80 kHz.

The stack tuner is connected to the transmission line via the coupling capacitor of a standard CVT. It consists of a series tuning inductor L_s and a parallel RLC network tuned the centre frequency of 80 kHz. The stack tuner is arranged so that it has a very high impedance at the power frequency (50 Hz) and is close to the line characteristic impedance at the tuned frequency (80 kHz). This is to minimise the attenuation at the tee point (Electricity Council,1981).

The line trap / stack tuner arrangement shown in Fig. 2 is connected to each of the three phases at each end of the teed circuit to be protected.

A NOVEL NON-UNIT PROTECTION SCHEME FOR EHV TEED TRANSMISSION CIRCUITS USING FAULT GENERATED HIGH FREQUENCY NOISE

BASIC PROTECTION STRATEGY

A fault on the power system will cause wide-band high frequency noise to be generated which will travel rapidly through the network due to the high propagation velocity of the travelling waves (slightly less than the speed of light). If the fault is internal to the network being protected there will be a relatively consistent signal around 80 kHz from the output of the stack tuner. If the fault is external then there will be severe attenuation of a very small band of high frequencies around the tuned frequency (80 kHz) due to the presence of the line trap and the busbar capacitance. Therefore discrimination can be achieved by comparing the signal strength close to 80 kHz with a reference signal.

PROTECTION SYSTEM

A block diagram of the protection system is shown in Figure 3. The system is made up of the following components.

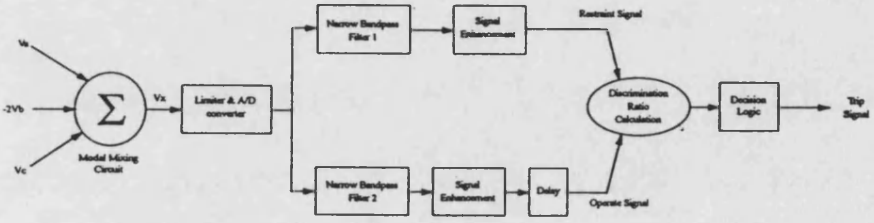


Fig. 3. Protection system

Modal Mixing Circuit

To reduce the amount of interference due to common mode signals being induced onto the line conductors the outputs from the three stack tuners are first combined to give two modal signals, which are

$$V_x = V_a - 2V_b + V_c \quad (4)$$

$$V_y = V_a - V_c \quad (5)$$

The first covers all faults except for an a-c phase fault and hence the need for the second mode.

Analogue to Digital Conversion

The modal signals are then digitised using a 12-bit A/D converter. This however creates a few problems due to the wide dynamic range of the signals that are expected to be received. For faults occurring close to a voltage maximum, the signals will be in the order of a few kilovolts, while for faults close to voltage zero they will be tens of volts. The quantisation step size is therefore set so that the lowest expected signals will have a digital level of about ten to minimise interference due to noise. This means however that the high signal levels have to be clipped which causes some distortion to the incoming signals. This is done by the signal limiter. In this paper the A/D converter limits the signals to ± 1024 V.

Narrow Bandpass Filters

These are used to extract the high frequency components from the modal input signals and are 6th order elliptic IIR filters. The first has a centre frequency of 78 kHz, fixed by the line trap / stack tuner centre frequency, and so is used for the 'operate' signal. The second has a centre frequency of 60 kHz and is used for the 'restraint' signal. This frequency was chosen to give the best possible output response.

Signal Enhancement

This is done by squaring the filter outputs and then passing them through a moving average window 1.25 msec long. Because the IIR filters have slightly different group delays, the 'operate' signal has to be delayed by 40 samples.

The discrimination ratio is calculated by dividing the 'operate' signal by the 'restraint' signal. For internal faults the ratio will be approximately equal to or greater than one, whereas it will be very close to zero for external faults. To provide extra security a counting regime has also been included and this is shown in Table 1.

TABLE 1 Decision Logic

Discrimination Ratio, Dr	Counter Increment
Dr > 0.8	+ 10
0.8 > Dr > 0.6	+ 9
0.6 > Dr > 0.4	+ 4
0.4 > Dr > 0.15	+ 1
0.15 > Dr > 0.1	- 1
0.1 > Dr > 0.005	-3
0.005 > Dr	- 10

When the discrimination ratio is greater than 0.15 the counter is incremented slowly and is incremented in larger steps as the ratio approaches one. If the ratio is less than 0.15, the counter is decremented slowly. As the ratio approaches zero the counter is decremented by larger amounts but its value is never allowed to fall below zero. When the counter reaches a value of 100 the trip signal is issued.

The counting regime is designed such that when the ratio is low, i.e. there is a small amount of uncertainty over the discrimination ratio due, for example, to noise, the counter is only incremented slowly. When the ratio is close to or above one, this gives a strong indication of an internal fault and so the counter is incremented more rapidly. This reduces the risk of the protection system issuing an incorrect trip signal for low ratios whilst ensuring a rapid trip when the ratio is close to or above one. The counter is devised such that it will always stay well below the required level of 100 for external faults, thus restraining tripping.

RESULTS

Internal Fault

Due to limitations of space only the results for single phase to earth faults are presented in this paper although the algorithm has also been tested for other fault types. All of the faults are applied 2.5 ms after the start of the simulations. Figures 4a-d show the results at end P for a voltage zero fault just in front of the line trap on the symmetrical tee network (Fig. 1a). The bursts of noise associated with the arcing can clearly be seen in Fig. 4a. In the frequency domain (Fig. 4b), the signal strengths at the two filter centre frequencies (i.e. 60 kHz and 78 kHz respectively) are comparable and this is confirmed by the discrimination ratio (Fig. 4c). In this case the decision logic issues a trip signal 0.35 ms after fault inception (Fig. 4d).

Figures 5a-d show the results for the same fault occurring at a voltage maximum. The high frequency noise signals this time have a much larger magnitude due to travelling wave effects (Fig. 5a). This signal therefore has to be limited during the quantisation process. The frequency domain plot of the stack tuner output again shows similar signal strengths at the two filter centre frequencies (Fig. 5b). The discrimination ratio rapidly rises above unity a very short time after the fault occurs (Fig. 5c) and the trip signal is issued 0.3 ms after fault inception (Fig. 5d).

External Fault

The results at end P for a voltage zero external fault on the busbar just behind the line trap on the same network are shown in Figs. 6a-d. The time domain signals (Fig. 6a) appear to be very similar to the internal fault case. However, in the frequency domain the blocking effect on the narrow band of frequencies around 80 kHz can clearly be seen (Fig. 6b). The discrimination ratio remains close to zero (Fig. 6c) and so the counter (Fig. 6d) stays at zero apart from one slight blip and this does not issue a trip decision due to the counting algorithm decision logic. Similar results are also obtained for a voltage maximum fault (Figs 7a-d). Although not presented here, the results from end Q and R are almost identical as the network is a symmetrical tee with equal source capacities.

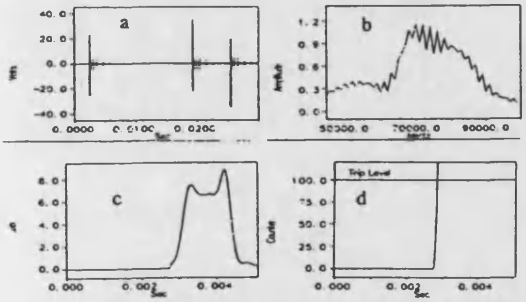


Fig. 4. End P internal voltage zero fault

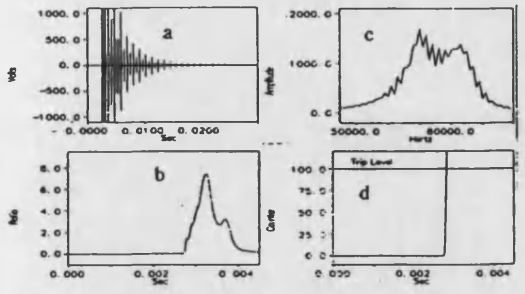


Fig. 5. End P internal voltage maximum fault

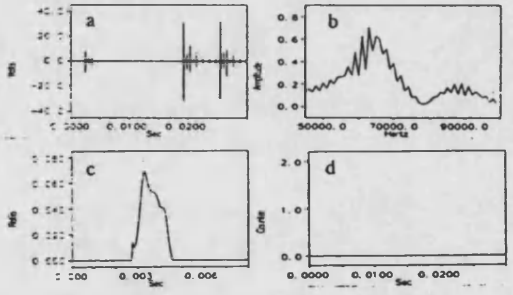


Fig. 6. End P external voltage zero fault

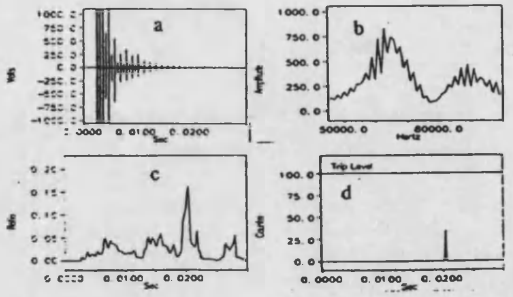


Fig. 7. End P external voltage maximum fault

Feed Around Paths

The ability of this protection algorithm to cope with feed around paths and line loading is demonstrated by applying a fault 10 km from end P on the unsymmetrical tee network (Fig. 1b) at a fault inception angle of 45°. The current outfeed at end R, due to the feed around path, can clearly be seen in Fig. 8a. The discrimination ratio and counter output for each of the ends (Figs.8b-g) indicate the algorithms correct evaluation of the fault and the trip signal is issued at each end 0.7 ms, 1.0 ms and 1.5 ms respectively after fault inception. The slight difference is due to the time it takes for the travelling waves to reach the line ends and the network effects, but is insignificant when compared to the likely circuit breaker operating times.

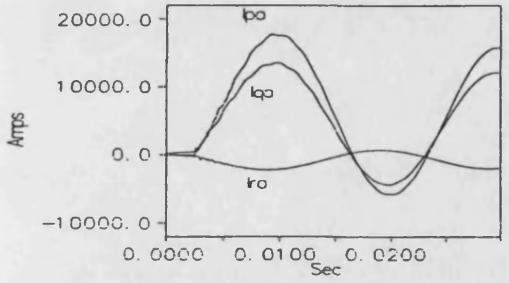
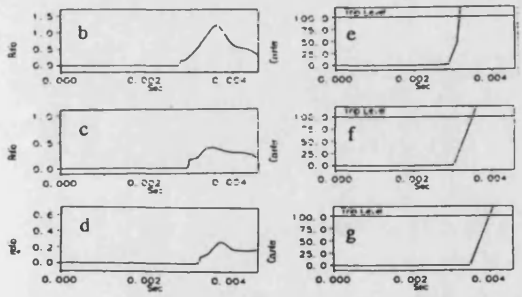


Fig.8a. Currents at each line end



Figs. 8b-g. Discrimination ratios and counter outputs for fault 10km from end P

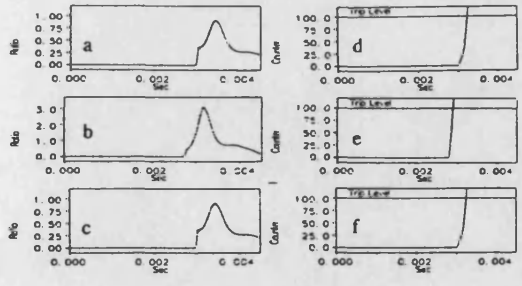


Fig. 9. Discrimination ratios and counter outputs for fault at tee point

Figures 9a-f show the results for a fault at the tee point at an inception angle of 45°. The fault is correctly identified and the trip signals are issued at end P, Q and R 0.75 ms, 0.4 ms and 0.75 ms respectively after fault inception.

This new technique is not significantly affected by the source side networks because the line trap presents a high impedance path to the high frequency signals causing the signals to be shunted through the busbar capacitance, which presents a very low impedance path to ground.

CONCLUSIONS

This paper clearly demonstrates how a new protection concept, based on capturing high frequency signals (generated by arcing faults) via conventional stack tuners and line traps, can be used to protect teed circuits. The major advantage of this technique lies in the fact that although it is a non-unit scheme, it possesses discriminatory properties associated with unit schemes. Furthermore, it is not adversely affected by such factors as feed around paths, infeed from the third terminal, unequal line lengths, etc.

ACKNOWLEDGEMENTS

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NON-UNIT PROTECTION OF EHV COMPOSITE CIRCUITS BASED ON FAULT GENERATED HIGH-FREQUENCY NOISE

A.M.Carter R.K.Aggarwal A.T.Johns Z.Q.Bo

Abstract

This paper describes a new technique for accurately detecting faults on EHV circuits containing overhead line and underground cable sections, using fault generated high frequency voltage signals. It is essentially a non-unit technique as it relies entirely on locally derived information but it has the discriminative properties normally associated with unit protection schemes. It does not need expensive communication channels which can compromise the security of some unit protection schemes if they fail. This new high speed digital relay uses a very fast sampling rate to capture the signals which are then manipulated using signal processing techniques. Simulated results are presented for a variety of internal and external faults. They show that the new relay is able to correctly discriminate between internal and external faults in less than approximately five milliseconds .

1 Introduction

Many transmission networks contain circuits which consist of overhead lines and underground cable sections. These *composite circuits* can be difficult to protect because of the large difference in the properties of overhead lines and underground cables. Distance protection relays can have problems because of the underground cables having a much higher impedance per unit length than the overhead line conductors and their sequence impedances are significantly different [1].

Compared with overhead lines, cables have a large shunt capacitance, significantly slower modal propagation velocities and a much greater attenuation rate [2]. However, short sections of cables are often found on EHV transmission systems. This may be because the circuit passes through an environmentally sensitive area or it is the most practical way to enter a substation.

Many papers have described different methods of modelling underground cable networks [3, 4], but little has been published on protecting them. Generally, they are protected using standard plain transmission line techniques with modified settings. The majority of conventional protection methods extract voltage and current information around the power system frequency to detect faults [5, 6]. Sudden changes in the power system voltage, caused by arcing faults for example, generate wideband high frequency (HF) signals on the associated EHV circuits [7]. These signals are generally outside the bandwidth of most voltage transducers.

This paper presents a technique for accurately detecting faults on composite circuits using these fault generated HF voltage signals. This is an extension of the work on protecting plain transmission lines and teed circuits [8, 9, 10]. The HF signals are captured with a specially designed stack tuner connected to a standard capacitor voltage transformer (CVT). Power line carrier (PLC) line traps are installed at each end of the circuit to be protected. Their bandstop filter characteristics are used to form a barrier between internal and external faults by confining the HF signals of interest to the protected zone. This scheme does not need any communication equipment as it relies solely on locally derived information. Therefore, it is a non-unit protection technique but it has the clearly defined boundaries associated with unit protection.

2 Signal Detection

The stack tuner and line trap arrangement used to capture the HF signals is shown in Fig.1. This is connected to all three phases at each end of the circuit being protected. A standard PLC line trap is used and is tuned to a specified centre frequency, f_c. Around f_c it offers a high impedance, blocking a narrow band of frequencies, and exhibits a low impedance at all other frequencies.

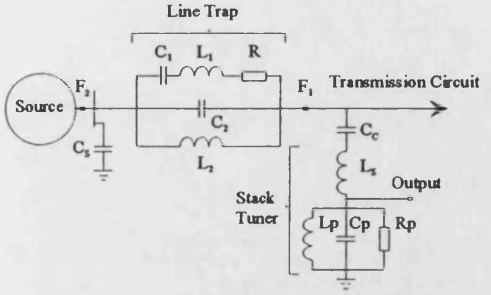

Fig. 1 - Line trap/stack tuner configuration

The line trap series resistance, R, is increased to approximately ten times the line characteristic impedance to improve the discrimination between internal and external faults. The stack tuner is connected to the coupling capacitor, C_c, of a standard CVT. At the power frequency, the stack tuner has a very high impedance and has an impedance close to the line characteristic impedance at f_c. The stray capacitance of the substation busbars is represented by C_s and a typical value of 0.1 μF is used. This also has the effect of strengthening the barrier between internal and external faults as it provides a low impedance path to ground for the high frequencies blocked by the line trap.

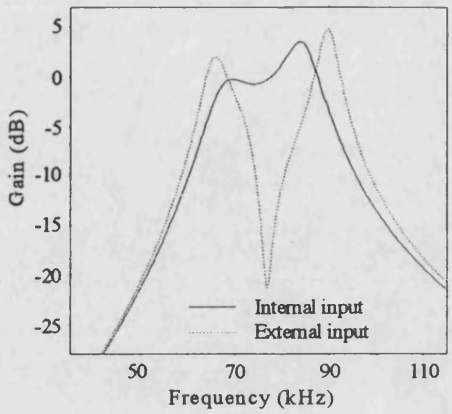

Fig.2 Frequency response of line trap/stack tuner

This is in contrast to an external disturbance at point F_2 in Fig.1. Here the 20 dB attenuation of a narrow band of frequencies around the centre frequency clearly shows the bandstop nature of the line trap.

3 Fundamental Operating Principle

The basic concept of this technique can be best understood by examining the frequency response of the line trap and stack tuner arrangement. For an internal disturbance at point F_1 in Fig.1, there is very little attenuation across the tuned band and increasing attenuation on either side [Fig.2].

The time domain stack tuner outputs are shown in Figs.3a and 3b for typical internal and external faults. This highlights the burst nature of the HF signals and shows that there is no significant difference between the waveforms. However, in the frequency domain, the effect of the line trap is clearly evident [Figs.3c,3d]. It is this difference that enables discrimination between internal and external faults to be achieved.

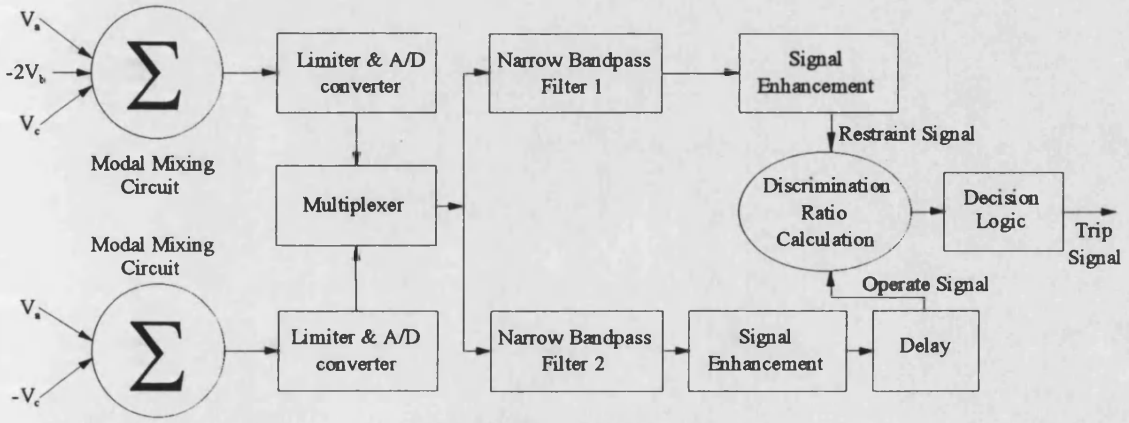

Fig.4 Protection system

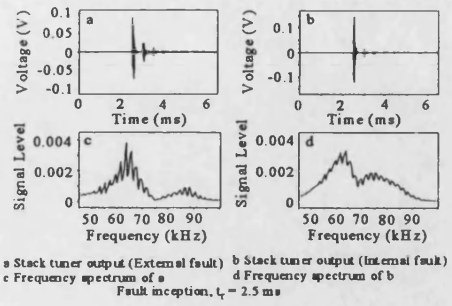

Fig.3 External and internal fault characteristics

A *discrimination ratio* is obtained by calculating a measure proportional to the spectral power at the centre frequency and then comparing it with the value at a slightly lower, reference frequency. For an internal fault, this ratio will be equal to or greater than unity and for an external fault it will approach zero.

4 Protection System

A block diagram of the protection system is shown in Fig.4. It is made up from a number of functional blocks and they are described below.

4.1 Modal Mixing Circuit

To avoid any problems caused by extraneous HF signals being superimposed onto the lines from adjacent power lines, or communication circuits for example, modal components are used. As the noise signals are normally associated with the earth, or common, mode, the two aerial modes are used. They are :

$$V_x = V_a - V_c \qquad (1)$$

$$V_y = V_a - 2V_b + V_c \qquad (2)$$

where V_x and V_y are the aerial mode voltages and V_a, V_b and V_c are the phase voltages.

4.2 Signal Limiting and A/D Conversion

Before the modal signals can be digitised, they need to be limited. This is because they have a very large dynamic range. Faults occurring close to a voltage maximum give rise to an initial HF burst of several kV. However, the bursts only have a magnitude of a few volts for faults near to a voltage zero. These differences are principally due to the amount of travelling waves created at the fault point.

The outputs from the stack tuners are first stepped down by an auxiliary transformer with a 200:1 turns ratio. In practice, this would be a specially designed wideband device with a radio metal core. An extensive series of computer aided design (CAD) studies have shown that clipping these signals to ± 10 V sufficiently reduces the required dynamic range without adversely affecting the schemes performance. The modal outputs are then formed and passed through a fourth order Butterworth anti-aliasing filter with a cut-off frequency of 100 kHz. A 12 bit analogue to digital (A/D) converter has been modelled to give the necessary precision.

A minimum threshold level of eight quantum levels is set within the software of the relay. This is to avoid problems due to spurious noise on the power system caused by corona discharge, electromagnetic interference or the thermal agitation of conductors for example.

4.3 Digital Filtering

Two digital narrow bandpass filters are used to extract the relevant high frequency signals from the quantised modal input signals. Sixth order elliptic infinite impulse response (IIR) filters are used as they have a very rapid transition between stop and pass bands with a minimum filter order. This has the advantage of minimising the group delay of the filters. The choice of the positions of the two filters is crucial to the correct operation of this protection scheme.

The *operate* filter frequency is fixed by the centre frequency of the line trap, in this case 75 kHz. The *restraint* filter frequency is chosen to give the best ratio for discrimination purposes. A large number of CAD studies were carried out and it was found that a *restraint* frequency of 61 kHz gave very good results, with both filters having a 2 kHz bandwidth.

4.4 Signal Enhancement

The filter outputs are enhanced by first squaring them and then averaging them over a 250 sample long moving window as shown in equation 3. This gives a signal proportional to the spectral power of the outputs.

$$Y(n\Delta t) = \frac{\sum_{k=n-L}^{n} V_{fx}(k\Delta t)^2}{L} \qquad (3)$$

where $Y(n\Delta t)$ is the enhanced output at time $n\Delta t$, n is the time step number, Δt is the time step (sampling interval), V_{fx} is the bandpass filter output and L is the length of the moving average window (250 samples ≡ 1.25 ms at 200 kHz sampling rate).

Because the two IIR filters have slightly different group delays, the operate signal has to be delayed by 40 samples to equalise them and so eliminate any phase shift errors. It is assumed that a high performance processor with floating point arithmetic would be used in the hardware implementation of the relay design. This removes the need to use scaling factors to avoid arithmetic overflow problems.

4.5 Discrimination Ratio and Decision Logic

The relay is able to distinguish between internal and external faults by calculating a *discrimination ratio*. This is calculated from the ratio of the enhanced operate filter output to the enhanced restraint filter output. For internal faults, this ratio will be approximately equal to or greater than one, whereas it will be very close to zero for external faults. In order to improve relay security, a counting regime has also been incorporated into the relay algorithm, and this is summarised in Table 1.

Table 1 - Counting Regime

Discrimination Ratio, D_r	Counter Increment
$D_r \geq 0.8$	+ 10
$0.8 > D_r \geq 0.6$	+ 9
$0.6 > D_r \geq 0.5$	+ 4
$0.5 > D_r \geq 0.4$	+ 1
$0.4 > D_r \geq 0.1$	- 1
$0.1 > D_r \geq 0.005$	-3
$0.005 > D_r$	- 10

Extensive CAD studies were carried out to determine the optimum settings of the counting regime and trip level. A trip level of 100 has been found to give a rapid relay trip for internal faults while the counter remains well below this level and restrains for external faults.

5 Relay Performance

The power system is simulated using the well proven EMTP software package and the protection system is simulated using offline C programs. Therefore, no allowance is made for the time taken for the microprocessor to perform the calculations. In practice these delays would be less than five milliseconds.

Due to the limitations of space, only typical results for single phase to earth faults and one mode, V_x are presented. The two configurations used in this paper are shown in Fig.5.

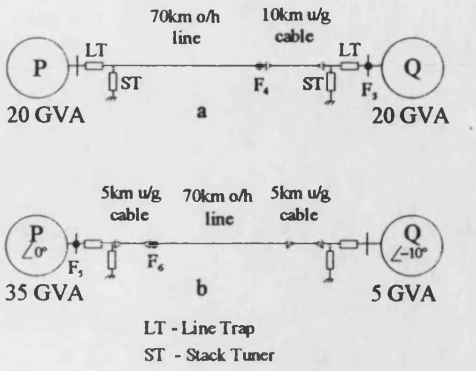

Fig.5 - Typical composite circuits

For an external fault occurring on the busbar at Q, F_3 in Fig.5a, at a voltage maximum, the results are shown in Fig.6. The time domain waveform (Fig.6a) shows the burst nature of the signals generated and the attenuation around the centre frequency of the line trap is clearly visible in the frequency domain waveform (Fig.6b). This gives a very low discrimination ratio (Fig.6c) and so the trip counter remains at zero (Fig.6d). Therefore, no trip output is generated as this is an external fault.

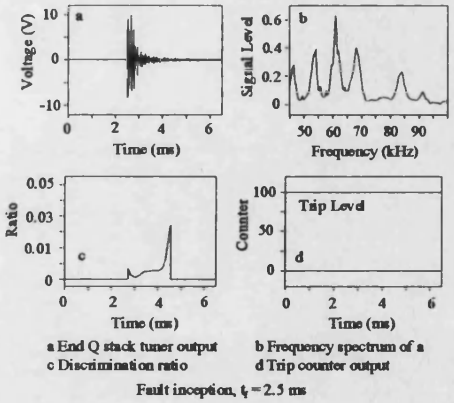

Fig.6 External Fault at F_3

An internal fault at F_4 in Fig.5a is shown in Fig.7. The fault is again at a voltage maximum. The time domain output (Fig.7a) shows a large initial burst and in the frequency domain (Fig.7b) some signal corruption is present. This is caused by the limiting of the input signal and the effect of the cable section. However, due to the positioning of the two bandpass filters, the discrimination ratio peaks at just above one (Fig.7c) and the trip counter exceeds the threshold level approximately 0.5 ms after fault inception (Fig.7d).

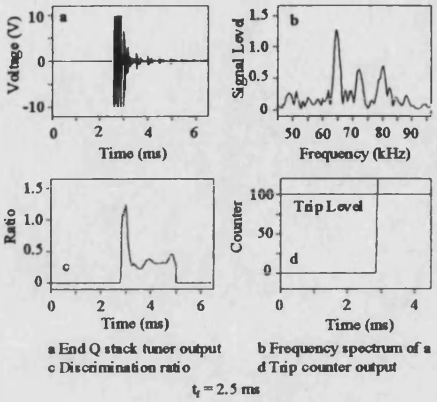

Fig.7 Internal fault at F_4

Figure 8 shows the discrimination ratios and trip counter outputs at both ends, for an external fault at the P end busbar (F_5 in Fig.5b). Here the source voltage at end Q lags P by 10° to represent some line loading and the fault occurs at an inception angle of 45° wrt end P. Both of the discrimination ratios remain close to zero (Figs.8a, 8b) and no trip decision is given (Figs.8c, 8d).

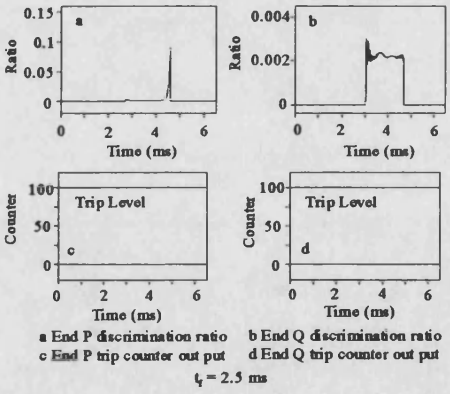

Fig.8 External fault at F_5

Using the same initial conditions as the last case, the fault is applied at F_6 in Fig.5b at an inception angle of zero degrees. Although only negligible travelling waves are produced,

this technique detects the HF signals generated by the arcing fault itself. The discrimination ratio peaks at approximately fifteen at P (Fig.9a) and at just below two at Q (Fig.9b). The trip counter exceeds the threshold at P 0.6 ms after t_f (Fig.9c) and at end Q 0.4 ms later (Fig.9d). This difference in time is due to the travel time of the HF signals along the conductors.

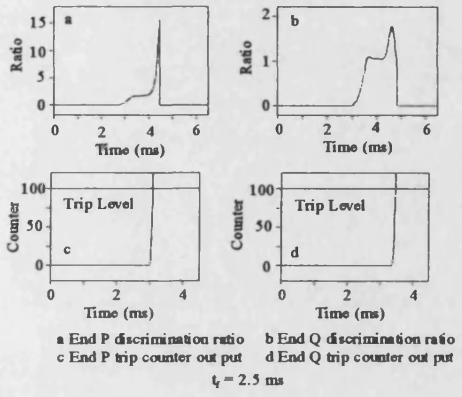

Fig.9 Internal fault at F_6

6 Conclusions

The results show that a technique based on fault generated high frequency noise can be used to protect EHV composite circuits. It is able to cope with different network and source configurations, as well as varying fault positions and inception angles. Internal and external faults can be typically identified in less than about five milliseconds. This is done using only locally derived information and so no expensive communication channels are required.

7 Acknowledgements

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COMPUTER-AIDED DESIGN OF A NEW NON-UNIT PROTECTION SCHEME FOR EHV TEED CIRCUITS

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Indexing terms: teed transmission circuits, non-unit protection, high frequency measurement

Abstract: This paper describes a new technique for protecting EHV teed transmission lines that is based on non-unit principles but exhibits the properties of a unit protection scheme. Fault generated high frequency (HF) signals are extracted from the coupling capacitor of a conventional capacitor voltage transformer (CVT) with a specially designed measurement circuit. Power line carrier line traps are used to confine the HF signals to the protected zone and their bandstop characteristics are used as a basis for discriminating between internal and external faults. A digital signal processing unit is used to process the signals and produce a trip output. Some simulated results are presented to show the scheme's ability to rapidly detect faults on different teed circuits under a variety of system and fault conditions encountered in practice.

1 INTRODUCTION

Teed circuits are likely to find widespread use on extra high voltage (EHV) transmission systems due to their significant economic and environmental advantages over two terminal lines. However, they can be difficult to protect using conventional techniques, particularly those that are based on non-unit principles. In this respect, it should be mentioned that although unit-protection schemes, such as Current Differential protection, have been successfully developed for such circuits [1], they require very reliable communication channels to avoid loss of integrity due to channel failure. In the case of non-unit schemes, the infeed into the tee point from the third terminal can pose serious problems in setting the reach of the very widely used Distance relays [2]. For protection relays based on travelling waves, reflections from the tee point impedance discontinuity coupled with those from the line terminations and the fault point can very significantly affect the distortion in the voltage and current waveforms detected at the line ends [3]. Many of these difficulties are compounded if the distances from the ends of the transmission lines to the tee point are significantly different from each other.

Conventional protection schemes generally rely on extracting voltage and current signals around the power system frequency to detect faults [4]. The wideband high frequency (HF) signals on EHV power lines created by a sudden change in the system voltage, due to travelling waves and arcing faults [5], are usually outside the bandwidth of most voltage transducers. Although much work

has been reported in the use of travelling waves for protection purposes, this has been largely confined to two terminal EHV lines and little has been reported on their application to teed feeders.

This paper describes an alternative technique for discriminatively detecting faults on teed circuits using the fault generated HF voltage signals measured at any one particular end. The fundamental principles are an extension of those reported in References [6,7] for two terminal lines. The HF signals are captured using a specially designed stack tuner connected to a standard capacitor voltage transformer (CVT). Power line carrier (PLC) signal line traps are used to confine the HF signals of interest to the protected zone and therefore form a barrier between internal and external faults. Consequently, this is a non-unit protection technique as it relies totally on locally derived information, but exhibits clearly defined boundaries associated with unit protection.

The main impetus of this paper is to describe specially developed digital signal processing techniques, as applied to the captured HF voltage signals, to effect a high speed protection technique for teed circuits for a vast majority of practically encountered system and fault conditions. The performance of the designed relay is demonstrated with reference to fault data generated on practical teed circuits comprising of 400 kV vertical construction lines of the type typically encountered on the British Supergrid system. The simulation of the fault data is based on the well known Electro-Magnetics Transient Program (EMTP) software.

2 SIGNAL DETECTION AND BASIC PRINCIPLES

The HF signals are detected by using the stack tuner and line trap arrangement shown in Fig 1 (this is essentially the same as described in ref[6]); this is connected to all three phases at each end of the transmission line being protected.

The line trap and stack tuner are tuned to the National Grid PLC Communication Band 1 (70-81 kHz) with a centre frequency of 75 kHz. The two tee circuit arrangements that are used to illustrate protection relay performance are shown in Fig 2.

The basic concept of the protection scheme has been fully described in ref[7]; briefly, based on the captured HF fault-generated signals, it involves forming two signals using digital filters: an *operate* signal based on signal energy around the centre frequency and a *restraint* signal based on signal energy slightly off-centre frequency. The ratio of these two signals determines whether the fault is in-zone or out-zone ie, a ratio close to or above unity indicates an internal fault and a ratio close to zero indicates an external fault. This ratio activates a counter which issues a trip decision when its value exceeds a predetermined threshold level.

3 POWER SYSTEM SIMULATION

The performance of this new protection scheme has been evaluated using the well proven EMTP software. A primary arc model, as has been developed in reference [8], is included in the simulations to represent the non-linear behaviour of the fault arc resistance.

The transmission lines simulated are

based on a single circuit of a typical quad-conductor 400 kV vertical construction overhead line of the type currently used on the British Supergrid system. The frequency dependence of the line parameters has been taken into account, a system frequency of 50 Hz is used and an earth resistivity of 100 Ωm is assumed. The source-side networks have been modelled using series lumped resistances and inductances to represent the short circuit capacities at the terminating busbars and an X:R ratio of 30 was assumed throughout. In order to conform with the *Nyquist theorem* and thereby prevent any aliasing errors, a sampling rate of 200 kHz was used in all the studies; as can be seen, this is greater than twice the maximum frequency of interest within the measured signals.

4 PROTECTION SYSTEM

A block diagram of the protection system is shown in Fig. 3. These operations are performed on the measured signals at each end of the teed circuit to give the trip indicators. Details of some of the processes are explained below.

4.1 Signal limiting and A/D conversion

The two modal signals (as described in ref[7]) have a large dynamic range. For example, for faults occurring near voltage maximum, there is a very large initial burst of HF signals of several kV, predominantly due to the presence of very significant travelling wave components that are associated with such faults. The net effect of this is that, at least during the initial very short period following a fault, the bursts of HF signals associated with the non-linear behaviour of the fault arc current get swamped by the very dominant travelling wave components. For faults near voltage zero on the other hand, the travelling wave components are virtually non-existent and the bursts of HF signals are predominantly due to the distortion caused by the non-linear arcing fault. These signals are much smaller than the previously mentioned travelling wave components.

If the data acquisition system (DAS) were to handle the complete range of signal levels, taking into account the factors just mentioned, then a resolution of more than 16 bits (this gives a very large signal-to-noise ratio) would be required. However, the most common type of analogue to digital (A/D) converter employed has a 12 bit resolution. This means that in order to retain relay sensitivity for a large majority of practically encountered faults, including those involving low level fault signals, it is necessary to reduce the dynamic range of the relay; this is achieved by *clipping* the analogue HF signals (particularly those associated with the aforementioned very large initial bursts) through a limiter, before conditioning them through an anti-aliasing filter, and digitising them through an A/D converter. A direct consequence of clipping is that for certain types of fault, there is some signal corruption with a loss of spectral power. However, as will be shown later, provided that the turns ratio of the auxiliary transformer within the DAS is carefully chosen such that the minimum levels of fault signals likely to be encountered in practice are always well above the spurious noise level admitted into the relay from the environment, corruption of high-level signals due to subsequent clipping does not adversely affect the performance of the relay. It should be mentioned that in practice, the auxiliary transformer is a specially designed wideband device comprising a

$$H(Z) = \frac{a_0 + a_1.Z^{-1} + a_2.Z^{-2} + a_3.Z^{-3} + a_4.Z^{-4} + a_5.Z^{-5} + a_6.Z^{-6}}{b_0 + b_1.Z^{-1} + b_2.Z^{-2} + b_3.Z^{-3} + b_4.Z^{-4} + b_5.Z^{-5} + b_6.Z^{-6}} \quad (1)$$

radio-metal core, with a typical turns ratio of 100:1 An extensive series of studies have shown that this ratio adequately covers the requisite dynamic range. The output signals from the transformer are limited to $\pm$10V, passed through an anti-aliasing, second-order Butterworth filter with a cut-off frequency of 100kHz, before being inputted into the A/D converter.

4.2 Circuit noise considerations

In practice, there can be spurious HF noise present on the system. This can be due to a number of factors such as corona discharge, thermal agitation of conductors, electromagnetic interference, etc. In this respect, studies have shown that the maximum level of background noise likely to be admitted into the DAS at the front end of the relay is typically about 40mV (as ascertained through some recent high voltage tests performed at the NGC's Laboratories at Leatherhead). This corresponds to 8 quantum levels based on a $\pm$10V, 12 bit A/D converter. A threshold set at this level within the relay software thus ensures that the relay is stable under healthy conditions, without its sensitivity being unduly affected for internal faults.

4.3 Digital filtering

The relevant high frequency components of the modal input signals are extracted with two digital narrow bandpass filters. Sixth order elliptic infinite impulse response (IIR) filters are used as they give a very rapid transition between stop and pass bands, with a minimum filter order, and therefore, minimum group delay. The choice of the filter centre frequencies is crucial to the correct operation of the protection scheme. The 'operate' filter frequency is fixed by the centre frequency of the line trap, in this case 75 kHz. The 'restraint' filter frequency is chosen to give the best ratio for discrimination purposes. To improve the scheme's performance further, a 2 kHz bandwidth filter was used at the 'operate' frequency of 75 kHz and a 1 kHz bandwidth filter at a 'restraint' frequency of 63 kHz. The Z-domain transfer functions of the filters are of the form shown in Eqn.1, where, a_n and b_n are the individual filter coefficients, and the frequency responses of these filters are shown in Fig. 4.

Care has to be exercised when fixing the word length of the filter coefficients as any loss in their precision can cause the filter pole positions to move slightly. This in turn may be sufficient to move the poles outside the Z domain unit circle, causing the filter to become unstable. It is thus vitally important to check this process very carefully; the risk of filter instability can be minimised by implementing each filter as a number of cascaded sections [9].

4.4 Signal enhancement

To give improved performance, the filter outputs are first squared and then averaged over a 250 sample (1.25 ms) long moving window. This gives a measure of the spectral energy content of

the signals (details are given in ref [7]).

4.5 *Discrimination ratio and decision logic*

The discrimination ratio is calculated from the ratio of the 'operate' signal to the 'restraint' signal. For internal faults, this ratio will be approximately equal to or greater than one, whereas it will be very close to zero for external faults. In order to improve relay security, a counting regime has also been incorporated into the relay algorithm, and this is summarised in Table 1.

Table 1 - Counting Regime

Discrimination Ratio, D_r	Counter Increment
$D_r \geq 0.8$	+ 10
$0.8 > D_r \geq 0.6$	+ 9
$0.6 > D_r \geq 0.5$	+ 4
$0.5 > D_r \geq 0.4$	+ 1
$0.4 > D_r \geq 0.1$	- 1
$0.1 > D_r \geq 0.005$	-3
$0.005 > D_r$	- 10

As can be seen from the table, when the discrimination ratio, D_r, is close to, or above one, the counter is incremented rapidly as the ratio gives a strong indication of an internal fault. When the ratio is between 0.6 and 0.4, the counter is incremented more slowly as there is some degree of uncertainty about the presence of an internal fault. The counter is decremented slowly, when the ratio falls below 0.4; finally, the counter is decremented rapidly, when the ratio is close to zero as this gives a strong indication of an external fault, but its value is never allowed to fall below zero.

Extensive CAD studies were carried out to ascertain the optimum settings of the counting regime and trip level. A trip level of 100 has been found to give a rapid relay trip for internal faults while the counter remains well below this level and restrains for external faults.

5 RELAY PERFORMANCE EVALUATION

5.1 *Internal faults*

Fig. 5 typifies the relay performance for an 'a'-phase-to-earth fault on the symmetrical tee network of Fig. 2a with equal source capacities at all three ends. The fault is applied when the 'a'-phase voltage is passing through 45^0, and the fault is at 25 km from end P, at point F_3. Due to limitations of space only the performance associated with aerial mode 'one' [7] is shown; the performance attained using aerial mode 'two' [7] is identical for the earth fault considered. The time domain responses of the unclipped and clipped stack tuner outputs at end P are shown in Figs. 5a and 5c respectively; their corresponding frequency spectra are shown in Figs. 5b and 5d. The first noise burst arrives a short time after fault inception because of the time taken for the signals to propagate along the transmission line from the fault point (see Figs.5a and 5c). The successive bursts are due to a combination of HF components generated by the non-linear behaviour of the primary fault arc and travelling wave components; these arise due to reflections from the impedance discontinuities in the

circuit such as at the fault point, the tee point and the line ends. As would be expected, in the case of signal clipping, Fig 5c shows that because the initial burst is limited to $\pm$10V (as compared to the unclipped signal for which the initial burst is in the range $\pm$70V as shown by Fig 5a), the magnitudes of the subsequent bursts appear to be relatively large. Although not shown here, the responses at ends Q and R are largely similar to those at end P.

In the frequency domain, the fairly consistent signal strength over the tuned band associated with the unclipped signals can be clearly seen from Fig 5b. Comparing these with the clipped signals shown in Fig 5d, the distortion and loss of spectral power due to clipping is apparent from the latter. However, although the signal clipping reduces the discrimination ratio (Fig.5e), it nevertheless is still well above the requisite level of 'one'; equally importantly, this level is maintained for approximately the same time period as that for the unclipped signals. The net effect is that the relay performance is practically unaffected by signal clipping, ie it initiates a trip decision in approximately the same time ($\approx$0.5 ms after fault inception) as that attained for the unclipped signals, as apparent from Fig 5f. It should be mentioned that this tripping time does not take into account any delays due, for example, to the processing times within the DAS, the calculation times within the floating point processor, etc; in practice these are likely to add a few ms to the overall relay operating time, but more importantly, the latter would still be $\leq$5 ms in a practical implementation of the technique.

It should be mentioned that the rest of the results presented herein are with the voltage limiter circuit incorporated within the protection scheme.

Figs 6a and 6c show the analogue HF relay signals for an 'a'-earth internal fault close to end P, at point F_1 on the system configuration shown in Fig 2a; the fault occurs near the minimum of the 'a'-phase voltage. In marked contrast to the previous case of a voltage maximum fault, the magnitudes of the HF bursts are very much attenuated and this is due to a distinct absence of any significant travelling wave components for such faults; the signal strength is largely dependent upon the distortion caused by the non-linear behaviour of the fault arc path. Moreover, as would be expected, there is no clipping of the signals and this effectively means that, unlike the previous case, there is no additional distortion of the signals (other than that caused by the primary system behaviour). As evident from the frequency spectra shown in Figs 6b and 6d at ends P and Q respectively, their waveshapes thus remain unchanged with little attenuation of spectral power at the centre frequency. The discriminant ratios thus exceed the requisite level of 'one' (see Fig 6e) and the relays assert trip decisions in approximately 1ms and 2ms at ends P and Q respectively; the additional delay associated with the end Q relay is as a direct consequence of the transit times involved in the HF components travelling from the fault point (which is near end P) to end Q. It should be noted that although not shown here, the end R relay performance is identical to that at end Q and this is so by virtue of the symmetry of the tee configuration used for this fault study.

Fig 7 illustrates the relay performance attained for an internal fault at point F_4 (25 km from end P) on the unsymmetrical teed circuit shown in Fig

2b; the fault is a 'b-c' phase fault clear of ground and occurs at point when voltage V_{bc} is passing through -120^0. As would be expected, because of the nature of this fault, HF bursts of fault signals are very much accentuated in comparison to the faults involving ground, as evident from Fig 7a. Moreover, signal clipping is also apparent and this manifests itself into some loss of spectral power and an additional signal distortion (see Fig 7b), but more importantly, the discrimination ratio rises above 'one' (soon after fault inception) at all three ends, as shown by Fig 7c. All the counter outputs exceed the required trip level very rapidly thereby correctly indicating an internal fault in less than about 1ms after fault occurrence (Fig.7d). Again no calculation delays are taken into account. It should be mentioned that for certain types of internal faults, the discriminant ratio can rise well above 'one' (as is the case here for end Q relay); this phenomenon, however, enhances relay performance rather than be detrimental to it.

5.2 *External faults*

Fig 8 typifies the relay performance for an external fault at F_2 on the symmetrical teed circuit shown in Fig 2a; the results are for a 'b-c' phase fault, when voltage V_{bc} is passing through -30^0. Here again, there is much HF activity and hence the levels of HF bursts are quite large; some clipping of the signals is thus inevitable as evident from Fig 8a. Fig 8b shows that in spite of an element of clipping, the characteristic feature of the frequency spectrum associated with an external fault, ie severe attenuation at around the centre frequency of 75 kHz, is retained. Although not shown here, this is also the case at ends Q and R. The net effect is that the discrimination ratios at all ends barely rise above a level of about 0.1 (see Fig 8c) and as a consequence, the counter outputs remain at zero as shown by Fig 8d.

The results presented in Fig 9 are for a typical 'a'-earth external fault near voltage zero of the 'a' phase voltage; this fault is also at point F_2 on the circuit shown in Fig 2a. As expected, the bursts of HF signals are sufficiently small so as not to be subjected to any clipping within the relay (see Figs 9a and 9c); like the previous case, the characteristic features of the signals, as apparent through the frequency spectra shown in Figs 9b and 9d, are very uniquely retained. Furthermore, the discrimination ratios remain well below 0.1 (see Fig 9e) and as a consequence, the relays restrain from operation at all three ends, as shown by Fig 9f.

Fig 10 is another example of the relay performance for an external fault, 40 km from end P on the feed around path of the unsymmetrical tee network (at point F_5 in Fig.2b). This is for an a-b-earth fault occurring when the 'a' and 'b' phase voltage magnitudes are equal (ie when the 'a' phase voltage is passing through -30^0). Here again, some degree of clipping occurs as is evident from Fig 10a but more importantly, there is very little deterioration in the quality of signals due to clipping as seen through the frequency spectrum of Fig 10b. At all three line ends, the discrimination ratio peaks at approximately 0.11 (Fig. 10c), and as this is well below unity, the counter outputs remain at zero and hence no trip decisions are indicated (Fig.10d).

6 CONCLUSIONS

This paper presents the computer-aided

design of a new protection scheme for use on EHV teed circuits. It relies entirely on locally derived information but has the discriminative properties associated with unit protection thus obviating the need for expensive and fallible communication channels. A specially designed stack tuner extracts HF signals via the high voltage capacitor of a standard CVT which are then fed into a digital signal processing unit. Digital filters are then used to extract the necessary information from these signals. A discriminative measurement can then be made by virtue of the internal and external fault HF signals exhibiting distinct characteristics.

The results presented show that the new scheme can distinguish clearly between internal and external faults on EHV teed circuits. A trip decision is issued in less than about 1ms after fault inception for all the different system and fault conditions studied; although in practice there would be some delays within the DAS and processor calculation delays, thereby adding to the relay operating time, the overall tripping times of the relay would still be ≤5ms for a vast majority of different system and fault conditions encountered in practice. A very important attribute of this technique lies in the fact that, within the practical limitations imposed by the signal-to-noise ratio of the A/D converter and the level of spurious noise present, it does not rely on the actual magnitudes of the HF fault signals received but on the relative magnitudes of the signals within the two characteristic frequency bands, once minimum fault signal pick-up levels have been exceeded; these levels are governed by the practical standing noise levels admitted into the relay hardware. Therefore, its performance is not influenced by factors such as fault position, fault inception angle, fault type, etc.

In addition, source and network configuration variations, including feed around paths, have no significant bearing on the scheme's performance in terms of giving correct discrimination between internal and external faults. This can be directly attributed to the line trap and busbar shunt capacitance forming a strong barrier between the circuit being protected and the rest of the power system. Furthermore, although for certain types of fault, the signal levels have to be clipped in order to accommodate a dynamic range covering a large variety of practically encountered faults, the relay performance is not unduly affected as a result of loss of signal power; these important attributes of the relay can be assigned to the robustness of the digital filter design and the incorporation of a sophisticated decision logic within the relay algorithm. This new technique, based on non-unit protection, is thus an important breakthrough in the protection of teed circuits which have hitherto found limited applications in situations where less than satisfactory protection performance is possible using non-unit techniques.

7 ACKNOWLEDGEMENTS

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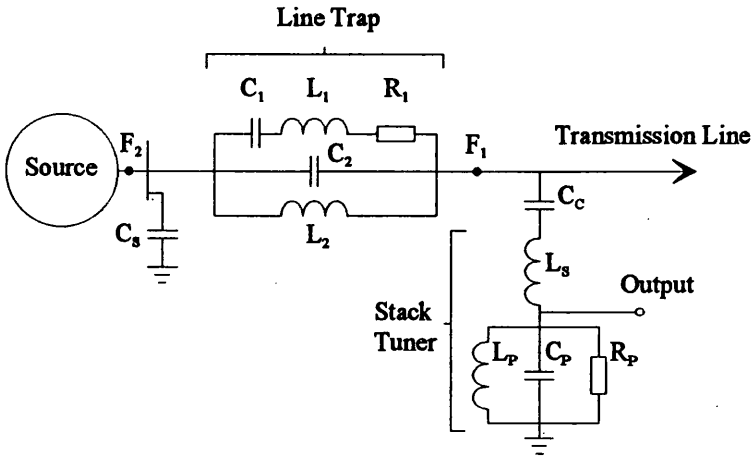

Fig.1 - Line trap / stack tuner arrangement

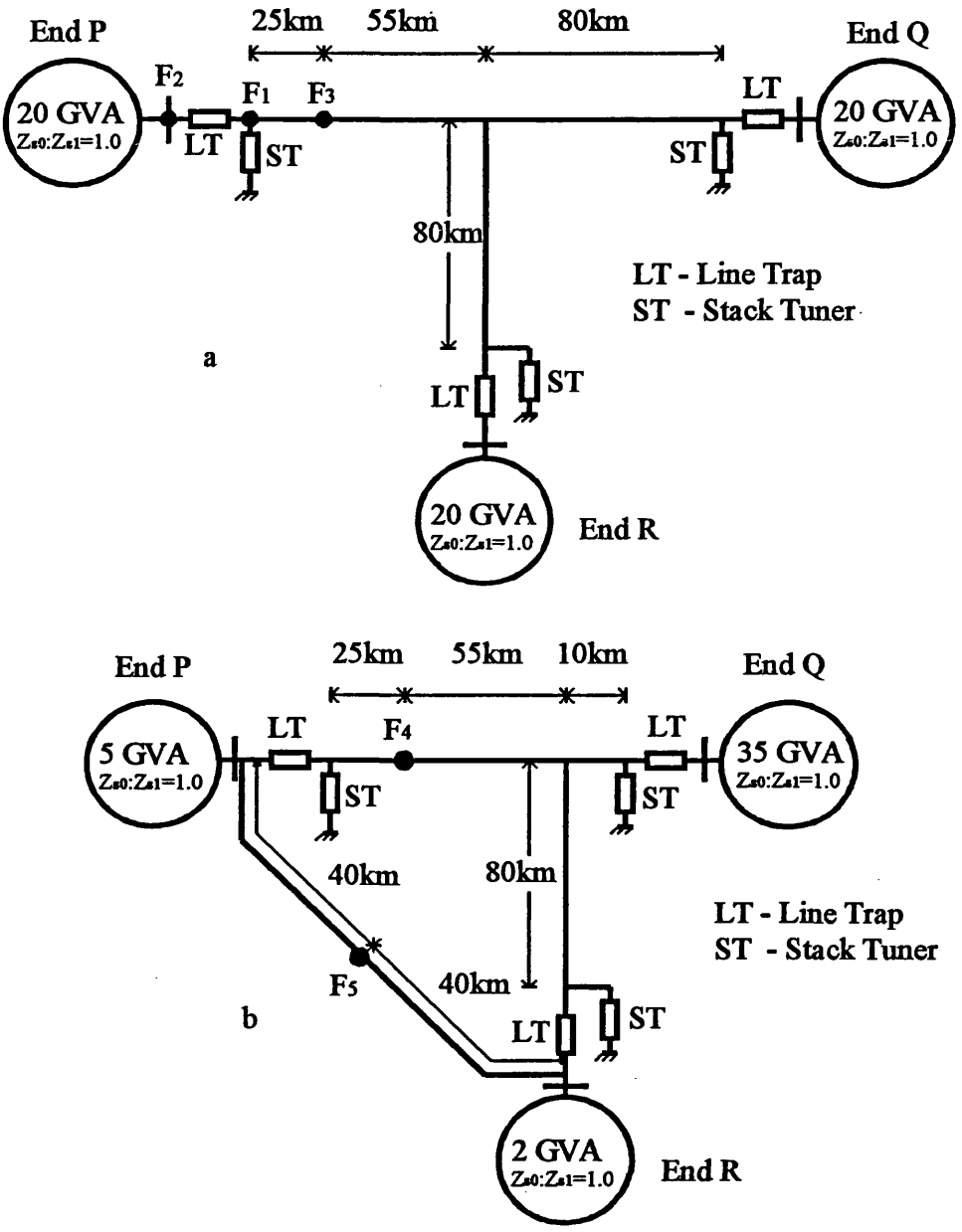

Fig. 2 Typical teed circuit configurations studied

a Symmetrical Tee

b Unsymmetrical Tee

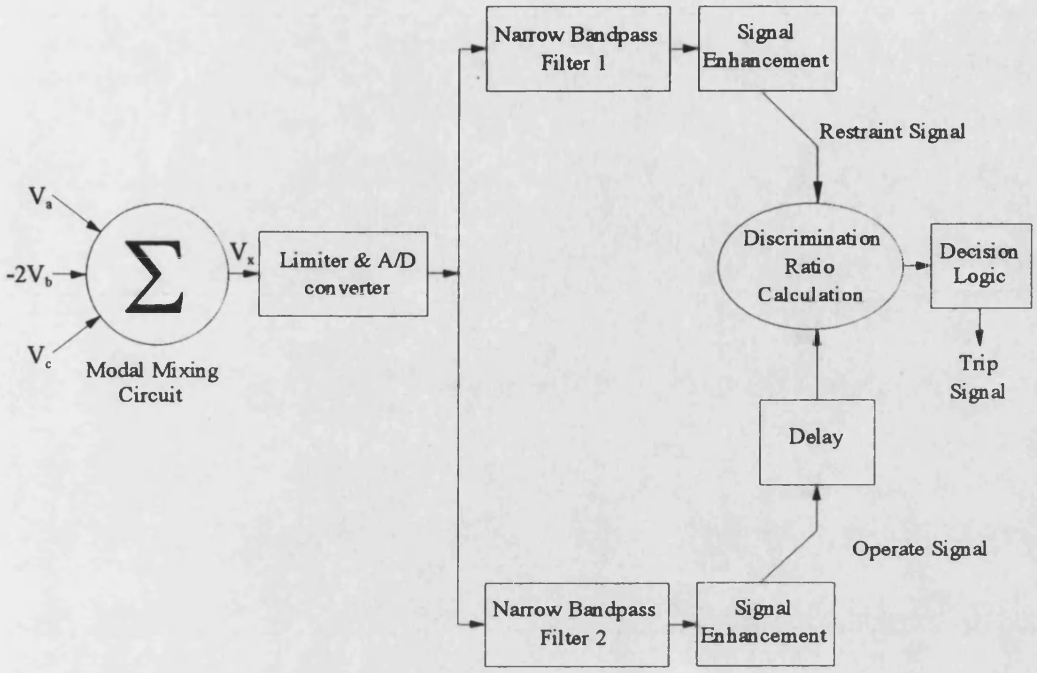

Fig.3 - Protection System

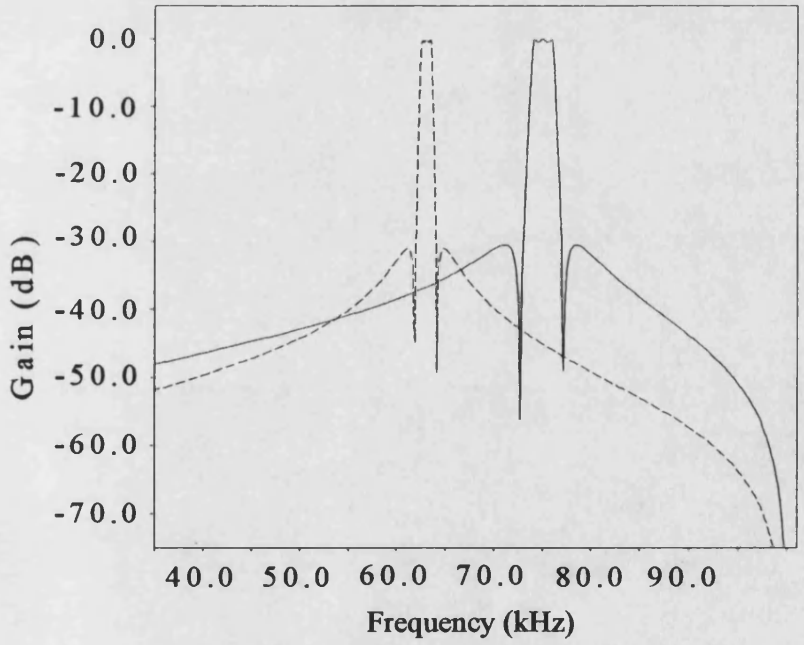

Fig. 4 Digital Filter Frequency Responses

—— Operate Filter

– – – Restraint Filter

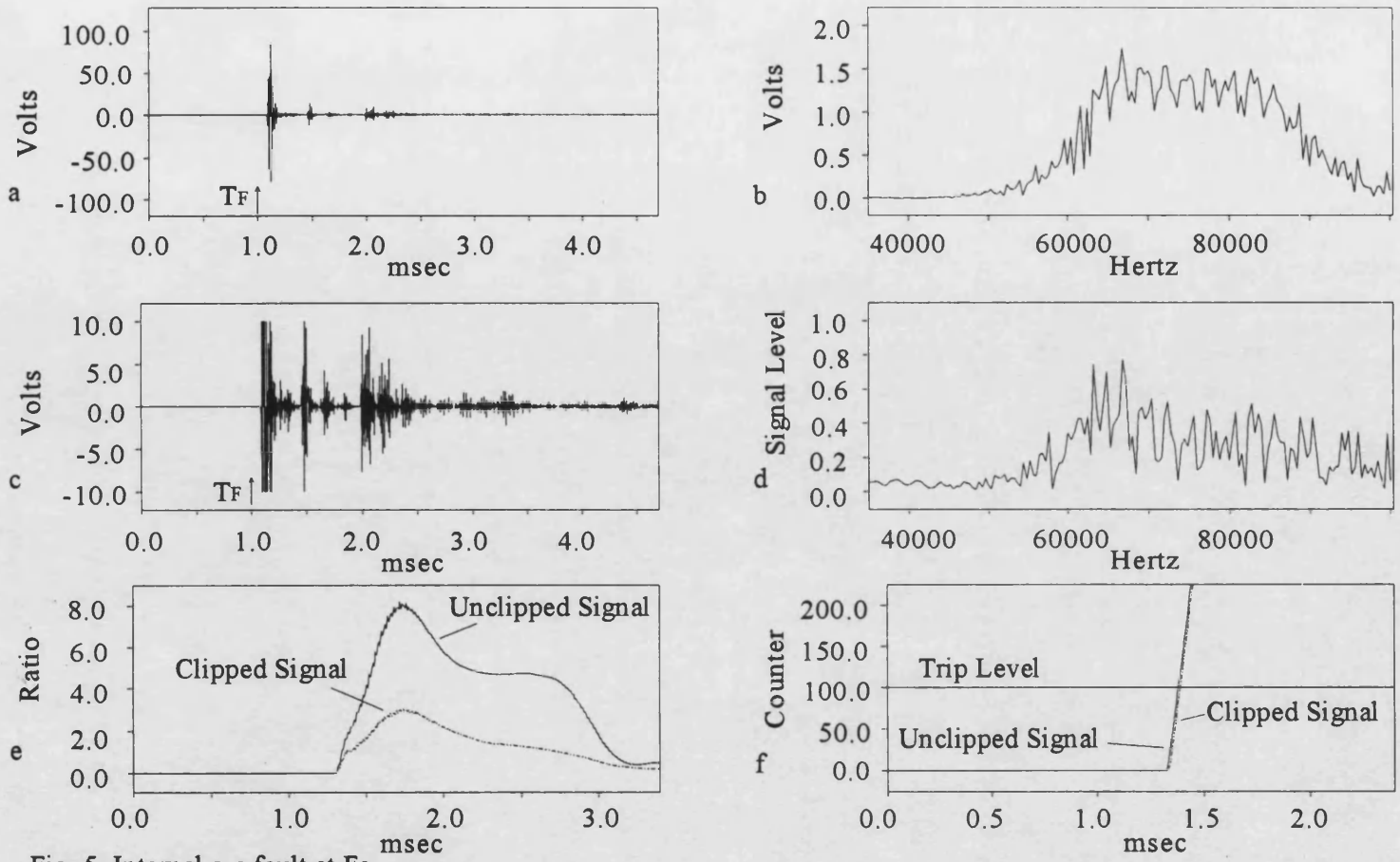

Fig. 5 Internal a-e fault at F_3
Symmetrical tee network (Fig.2a)
Fault applied at 45deg after 1ms
T_F - Fault inception time

a Unclipped end P stack tuner voltage
b Frequency spectrum of unclipped signal
c Clipped end P stack tuner voltage
d Frequency spectrum of clipped signal
e Discrimination ratios
f Counter outputs

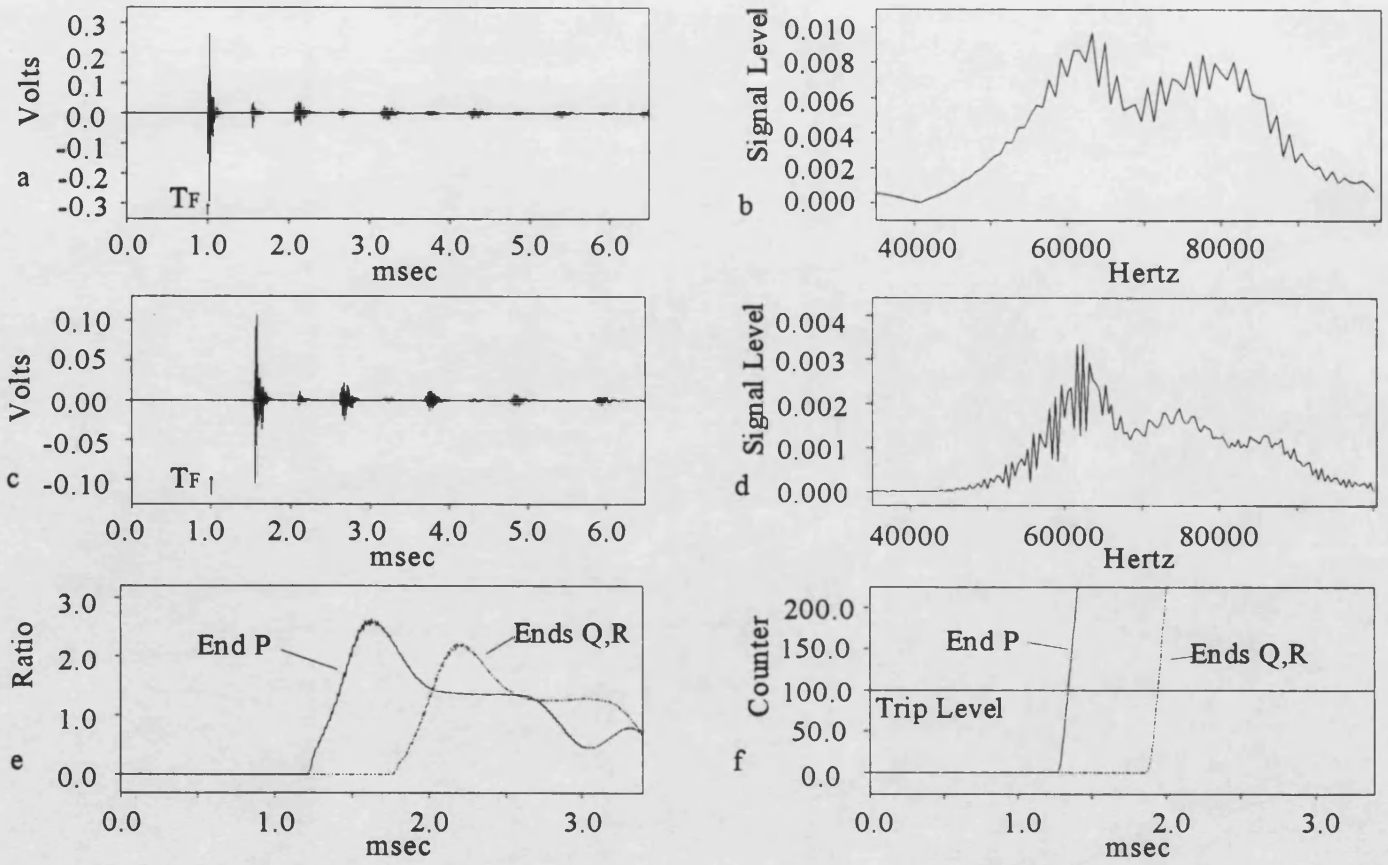

Fig. 6 Internal a-e fault at F_1
Symmetrical tee network (Fig.2a)
Fault applied near voltage zero after 1 ms
T_F - Fault inception time

a End P stack tuner voltage
c End Q stack tuner voltage
e Discrimination ratios

b End P frequency spectrum
d End Q frequency spectrum
f Counter outputs

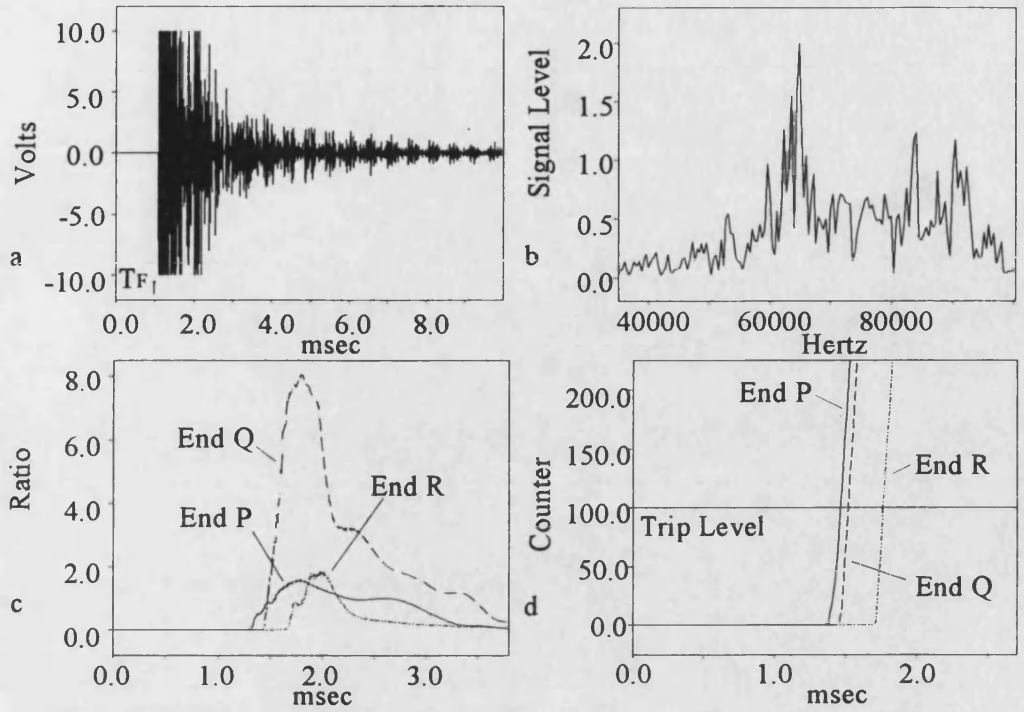

Fig. 7 - Internal b-c phase fault at F_4 Fault applied at 180deg wrt phase c after 1ms
Unsymmetrical tee network (Fig.2b) T_F - Fault inception time
a End P stack tuner voltage b End P frequency spectrum
c Discrimination ratios d Counter outputs

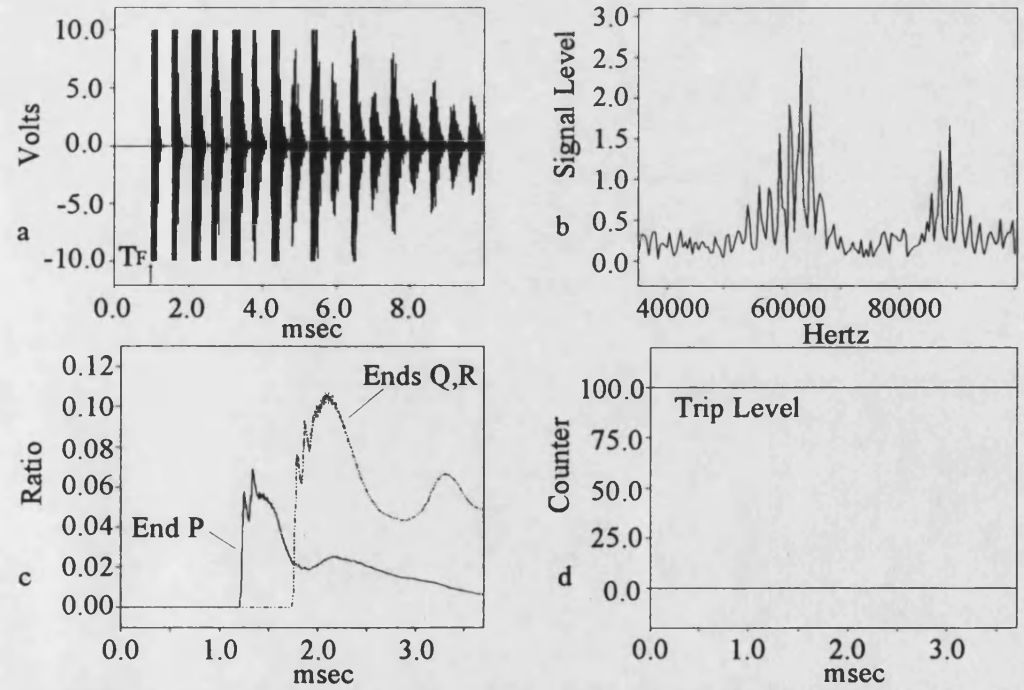

Fig. 8 External b-c phase fault at F_2 Fault applied at 180deg wrt phase c after 1ms
Symmetrical tee network (Fig.2a) T_F - Fault inception time
a End P stack tuner voltage b End P frequency spectrum
c Discrimination ratios d Counter outputs

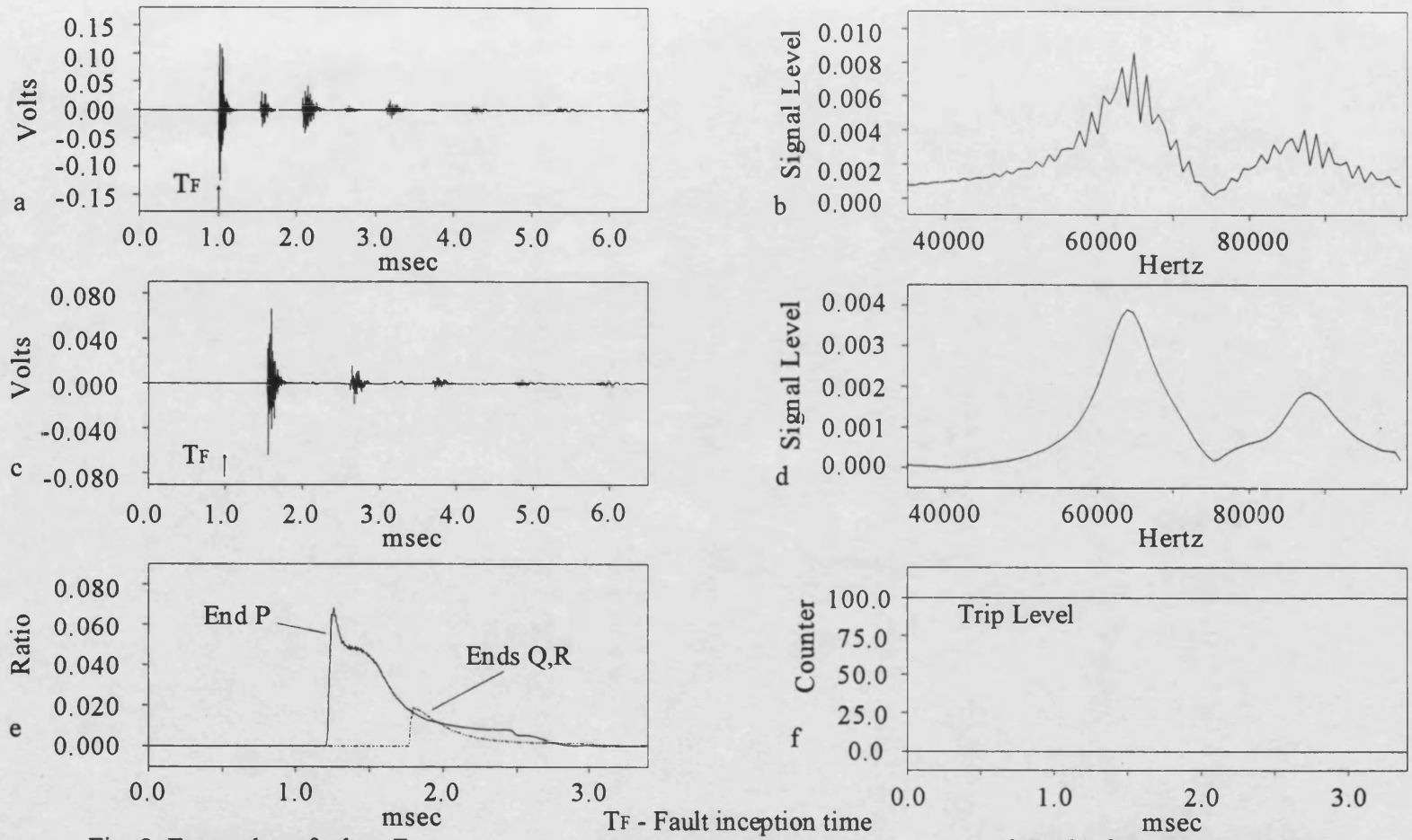

Fig. 9 External a-e fault at F 2
Symmetrical tee network (Fig.2a)
Fault applied near voltage zero after 1ms

TF - Fault inception time
a End P stack tuner voltage
c End Q stack tuner voltage
e Discrimination ratios

b End P frequency spectrum
d End Q frequency spectrum
f Counter output

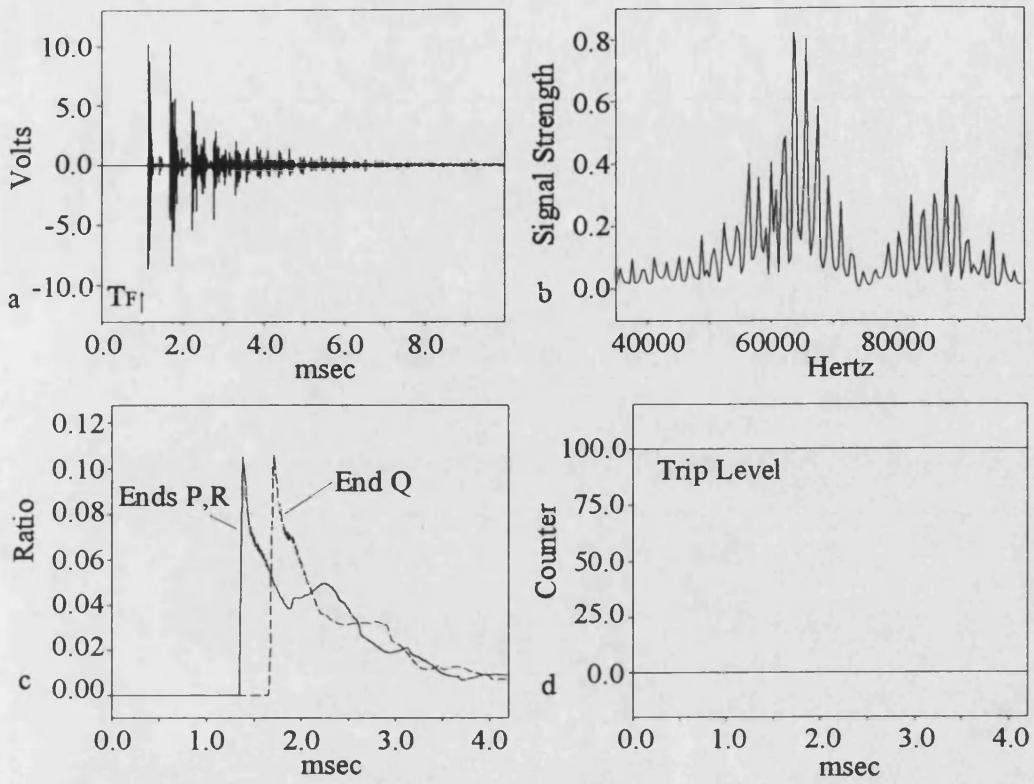

Fig. 10 External a-b-earth fault at F5 Fault applied at -30deg wrt phase a after 1ms
Unsymmetrical tee network (Fig.2b) TF - Fault inception time

a End P stack tuner voltage b End P frequency spectrum
c Discrimination ratios d Counter outputs